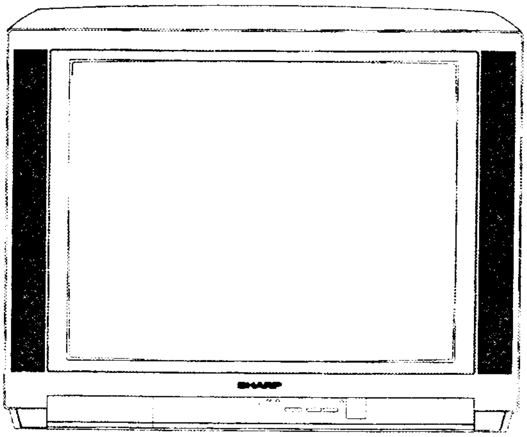
SHARP SERVICE MANUAL

SEMJ70ES04S//

CA10- CHASSIS



PAL SYSTEM COLOUR TELEVISION

MODEL 70ES-04S

In order to service model 70ES-04S, refer to the previously issued Service Manual for model 70DS-03S. This manual only contains the differences beween the above mentioned models.

In the interests of user-safety (required by safety regulations in some countries) the set should be restored to its original condition amd only parts identical to those specified should be used.

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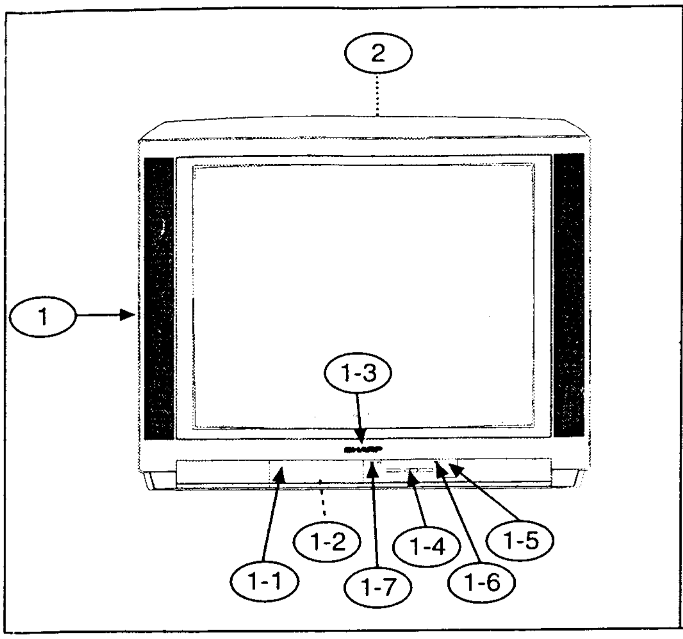
- PARTS LIST 2

SHARP CORPORATION

70ES-04S

The difference between the previous model 70DS-03S and the current model 70ES-04S, is only the cabinet.

PARTS LIST (Only contains the differences)



REF. NO.	PARTS	★	DESCRIPTION	CODE
			MISCELLANEOUS PARTS	
	TINS-6577BMNO	S	Operation Manual	AR
			CABINET PARTS	
1	CCABA1228BMV0	S	Front Cabinet	BF
1-1	GDORF1052BMSA	S	Door	AE
1-2	PKAI-1083BM00	S	Door Latch	AF
1-3	HBDGB3013MESB	S	Badge SHARP	AH
1-4	JBTN-1049BMSA	S	Button Up/Down	AD
1-5	JBTN-1048BMSA	S	Button Power	AD
1-6	HDECQ0037BMSA	S	Window Power	AC
1-7	HDECQ0038BMSA	S	Window	AC
2	CCABB1083BMV0	S	Rear Cabinet	BE

SHARP

RECICLED PAPER

PRINTED IN SPAIN

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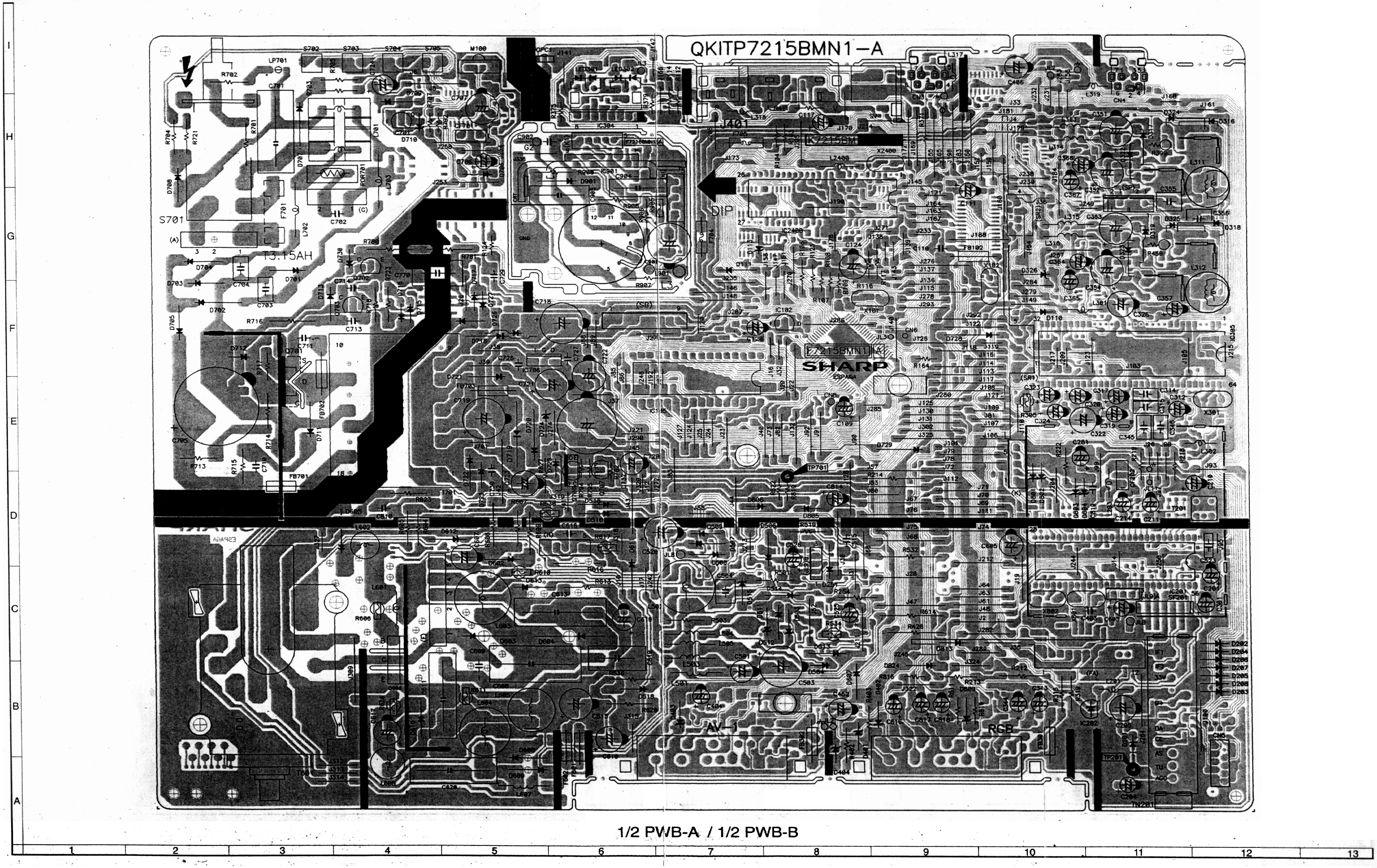
PRINTED WIRING BOARDS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J401
K7215BM
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SHARP
ESPAÑA
DIP
T3.15AH
S701
AV-1
RGB
TP701
TP201
TN201
CN4
CN5
CN8
IC301
IC304
IC102
IC2400
IC202
X2400
X301
F701
PCR701
FB701
FB702
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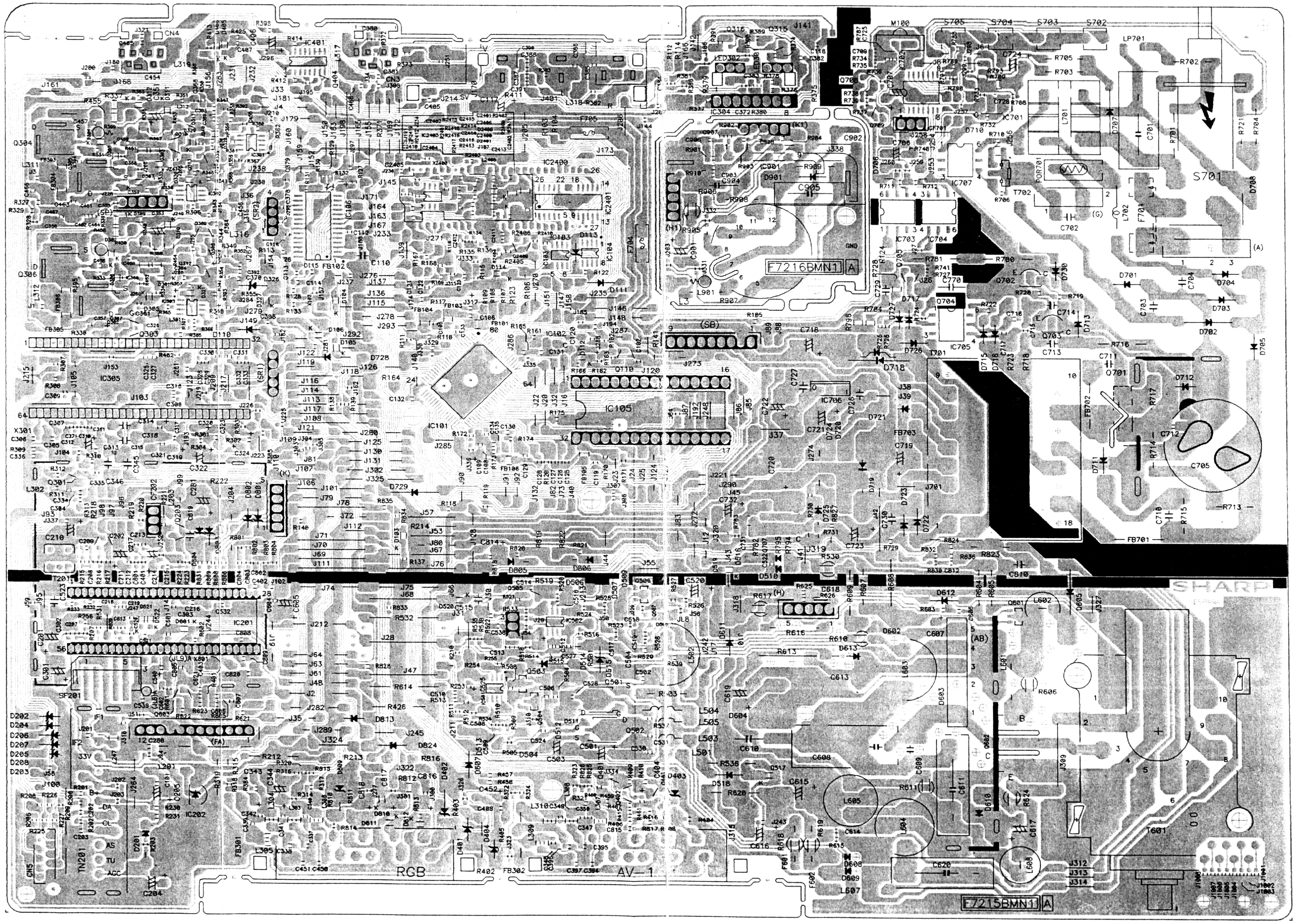
1/2 PWB-A / 1/2 PWB-B

PRINTED WIRING BOARDS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F7215BMN1 A
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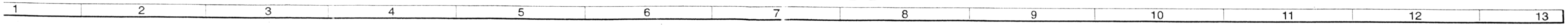
AV-1
S701
IC101
IC105
IC2400
IC201
IC202
T601
T701

1/2 PWB-A / 1/2 PWB-B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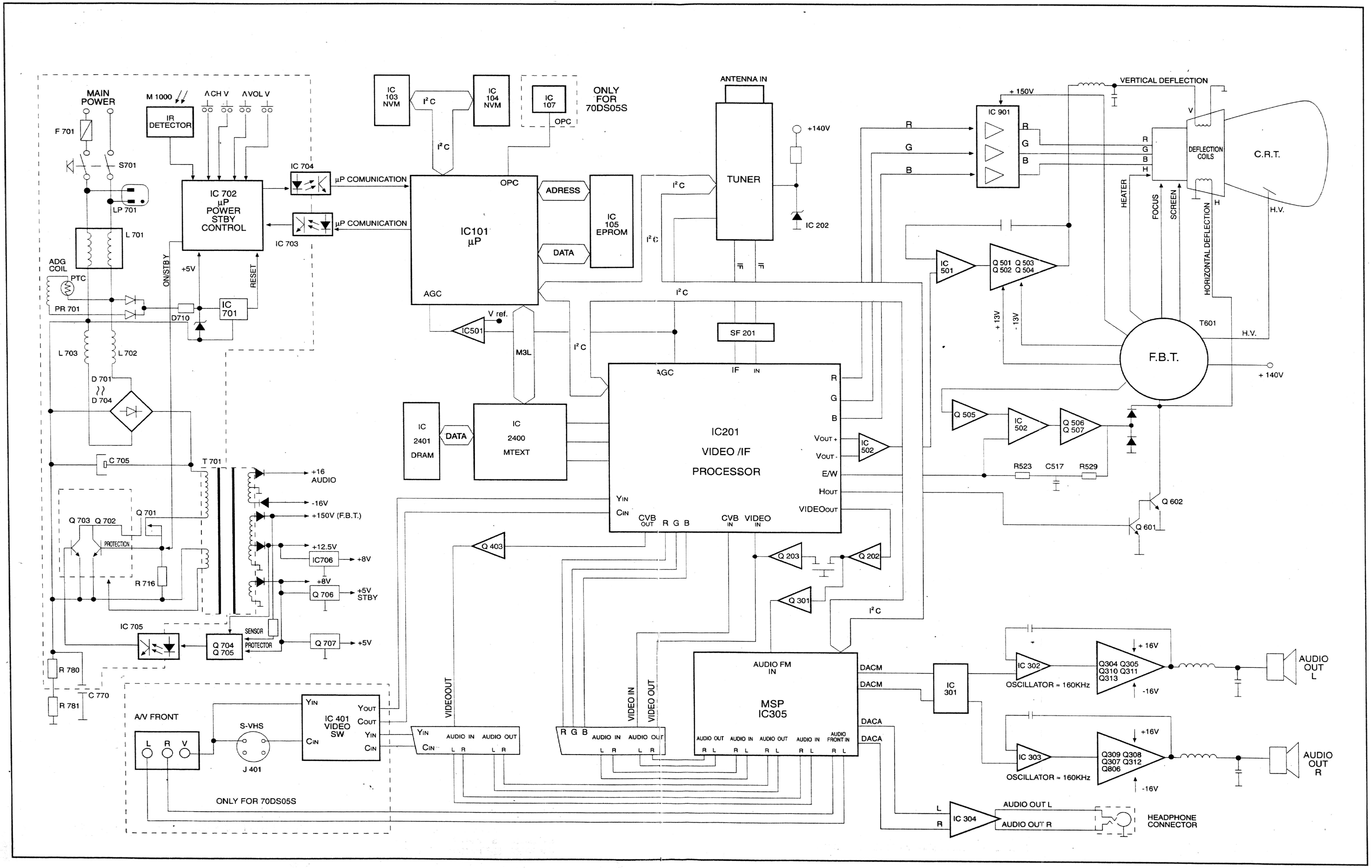
BLOCK DIAGRAM 63DS03S / 70DS03S / 70DS05S


MAIN POWER
F 701
S701
LP 701
L 701
ADG COIL
PTC
PR 701
D710
L 703
L 702
D 701
D 704
C 705
T 701
Q 703 Q 702
Q 701
PROTECTION
R 716
IC 705
R 780
R 781
C 770
M 1000
IR DETECTOR
Λ CH V
Λ VOL V
IC 702 µP POWER STBY CONTROL
ON/STBY
+5V
RESET
IC 701
IC 704
IC 703
µP COMUNICATION
µP COMUNICATION
+16 AUDIO
-16V
+150V (F.B.T.)
+12.5V
IC706
+8V
+8V
Q 706
+5V STBY
SENSOR PROTECTOR
Q 704 Q 705
Q 707
+5V
A/V FRONT
L R V
S-VHS
J 401
IC 401 VIDEO SW
YIN
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YOUT
COUT
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ONLY FOR 70DS05S
IC 103 NVM
I²C
IC 104 NVM
I²C
IC 107
OPC
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IC101 µP
OPC
AGC
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DATA
IC 105 EPROM
V ref.
IC501
M3L
IC 2401 DRAM
DATA
IC 2400 MTEXT
ANTENNA IN
TUNER
+140V
IC 202
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I²C
I²C
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SF 201
I²C
IC201 VIDEO /IF PROCESSOR
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E/W
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VIDEOOUT
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CVB OUT
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VIDEO IN
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Q 202
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MSP IC305
AUDIO OUT
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AUDIO OUT
AUDIO IN
AUDIO FRONT IN
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DACM
DACA
DACA
IC 502
+150V
IC 901
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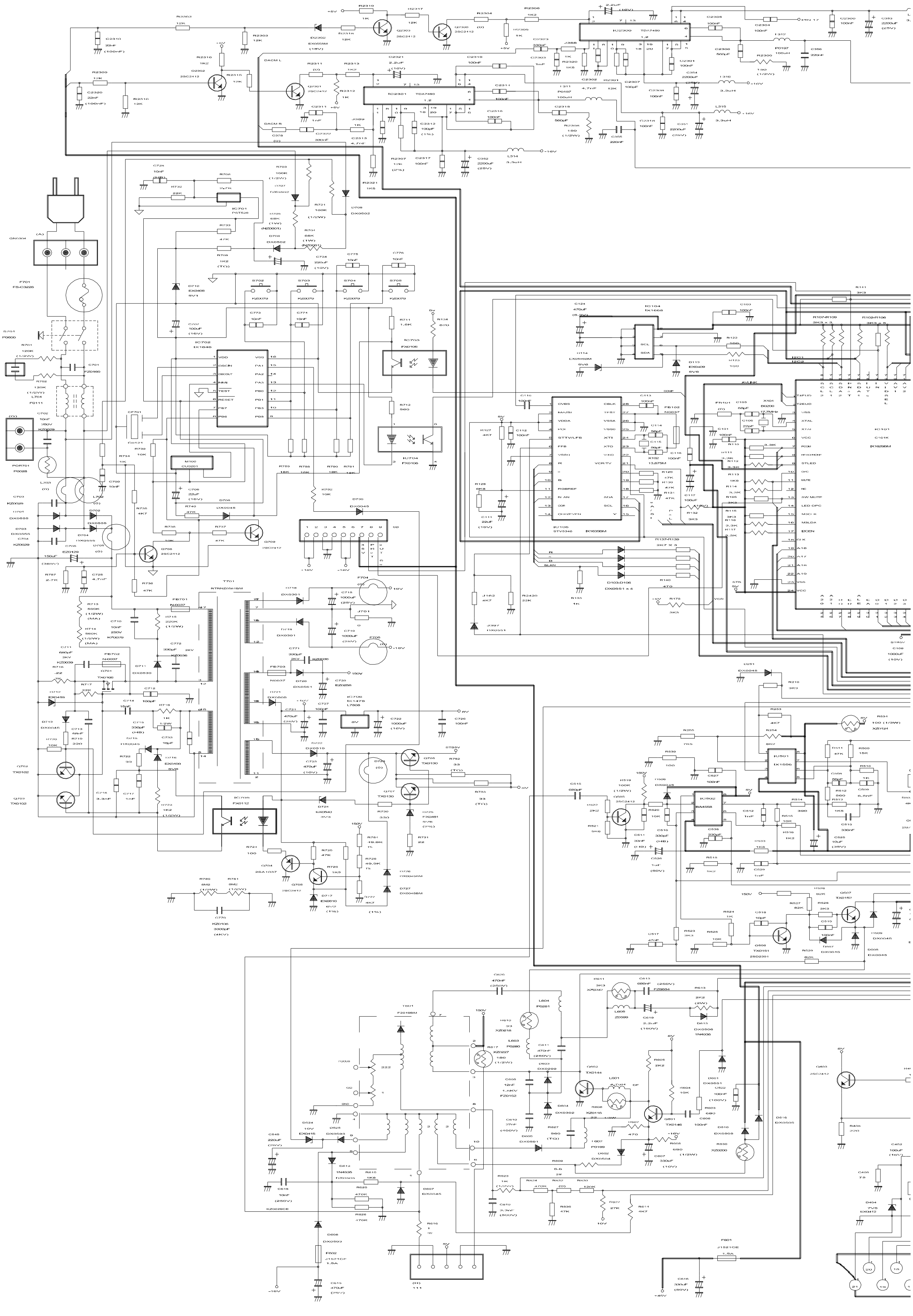
VERTICAL DEFLECTION
V
DEFLECTION COILS
C.R.T.
H
HEATER
FOCUS
SCREEN
HORIZONTAL DEFLECTION
H.V.
IC 501
Q 501 Q 503
Q 502 Q 504
+ 13V
- 13V
T601
F.B.T.
H.V.
+ 140V
Q 505
IC 502
Q 506 Q 507
R523
C517
R529
Q 602
Q 601
IC 301
IC 302
OSCILLATOR ≈ 160KHz
Q304 Q305
Q310 Q311
Q313
+ 16V
-16V
AUDIO OUT L
IC 303
OSCILLATOR ≈ 160KHz
Q309 Q308
Q307 Q312
Q806
+16V
-16V
AUDIO OUT R
IC 304
L
R
AUDIO OUT L
AUDIO OUT R
HEADPHONE CONNECTOR

SCHEMATIC DIAGRAM.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DACM R
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IX1068
IC106
STV5346
IC101
IC501
IC502
T701
T801
F701
LP701
PCR701
Q702
Q703
Q704
Q705
Q706
Q707
Q708
Q709
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150V
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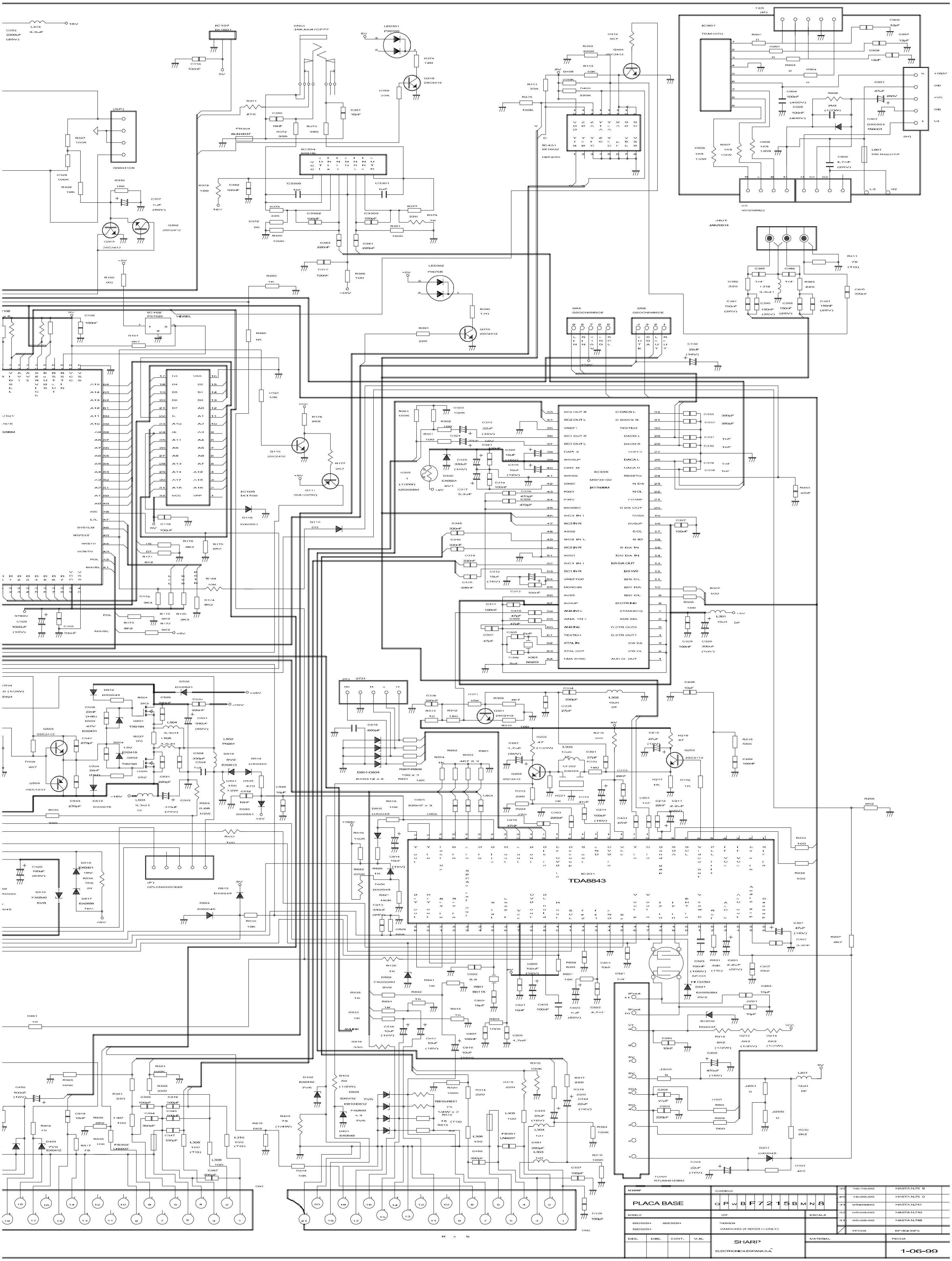
8V


IC201
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IC305
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IC401
HEF4053
IC901
IC102
IC105
IC107
TU201
RTUNH0123BM
J401
JAK20014
SRA
SRB
CN1
CN2

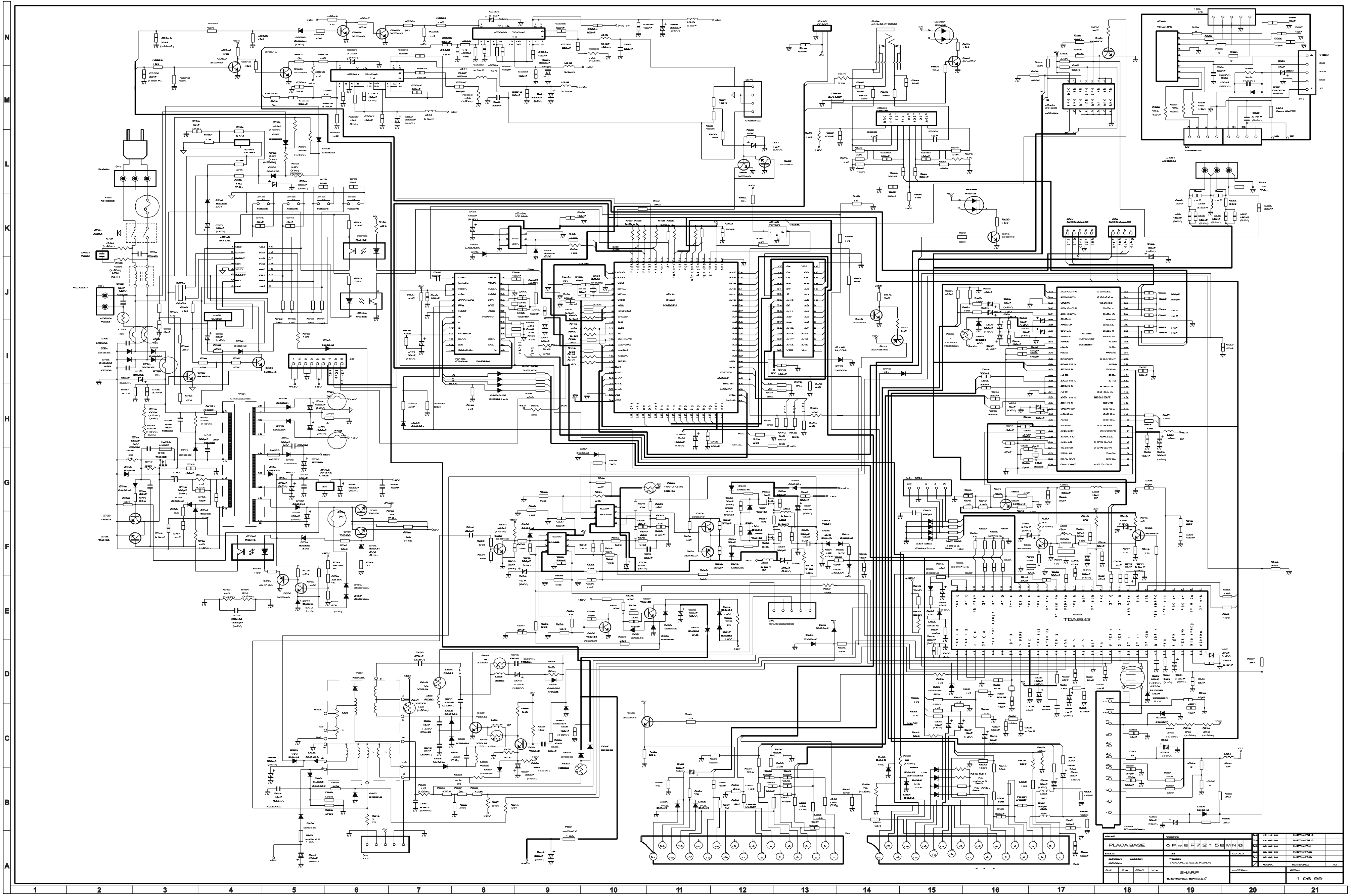
NOMBRE	CODIGO			
PLACA BASE	QPwBF7215BMN8			
MODELO	CRT	ESCALA		
66DS05H 66ES05H 59DS05H	THOMSON SAMSUNG (59DS05H ONLY)			
DIS.	DIB.	CONT.	V.B.	

SHARP
ELECTRONICA ESPAÑA S.A.

	FECHA	REVISIONES
30	10-10-00	HASTA N.75 9
29	18-09-00	HASTA N.75 0
33	05-09-00	HASTA N.741
32	05-09-00	HASTA N.740
31	05-09-00	HASTA N.748

MATERIAL	FECHA
	1-06-99

SCHEMATIC DIAGRAM.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59DS-05H
66DS-05H
66ES-05H

SCHEMATIC DIAGRAM.

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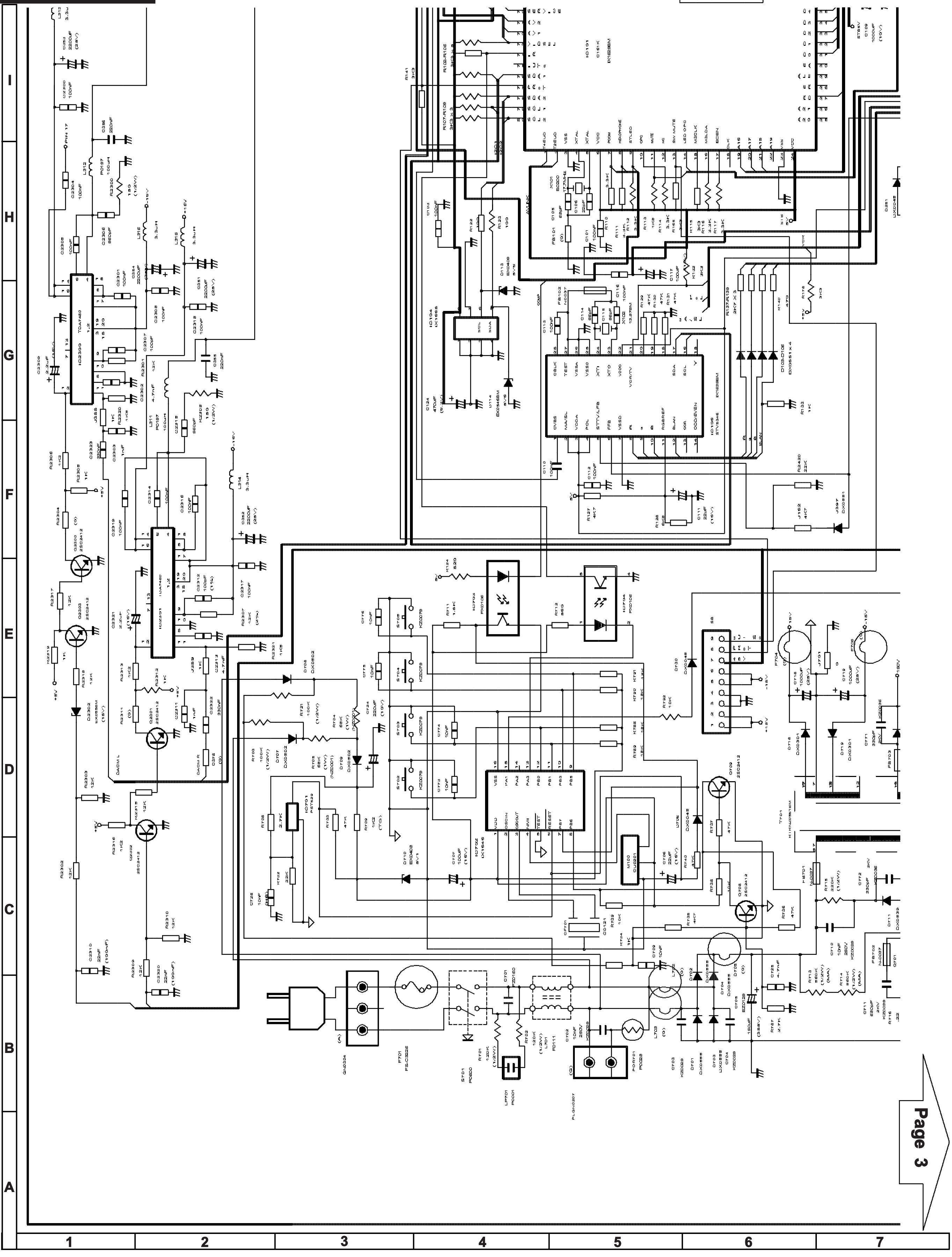
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IC2300
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TDA7480
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IC104
IX1565
IC702
IX1646
IC701
PST529
M100
Q2300
2SC2412
Q2301
2SC2412
Q2302
2SC2412
Q703
2SC2412
Q708
2SC2412
T701
F701
S701
L701
+5V
+16V
DACM L
DACM R

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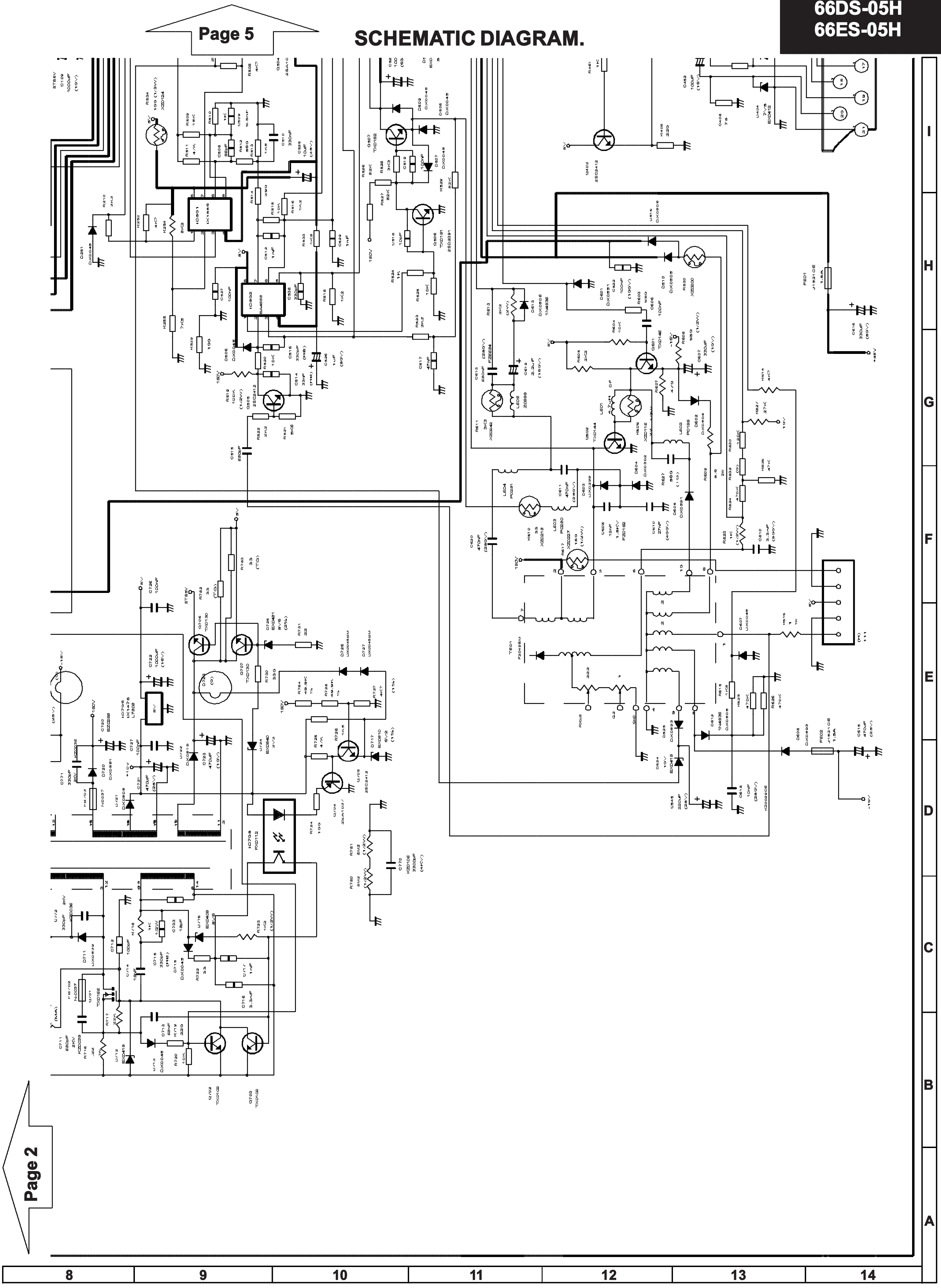
59DS-05H
66DS-05H
66ES-05H

SCHEMATIC DIAGRAM.



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IC801
IC802
IC705
T601
FE01
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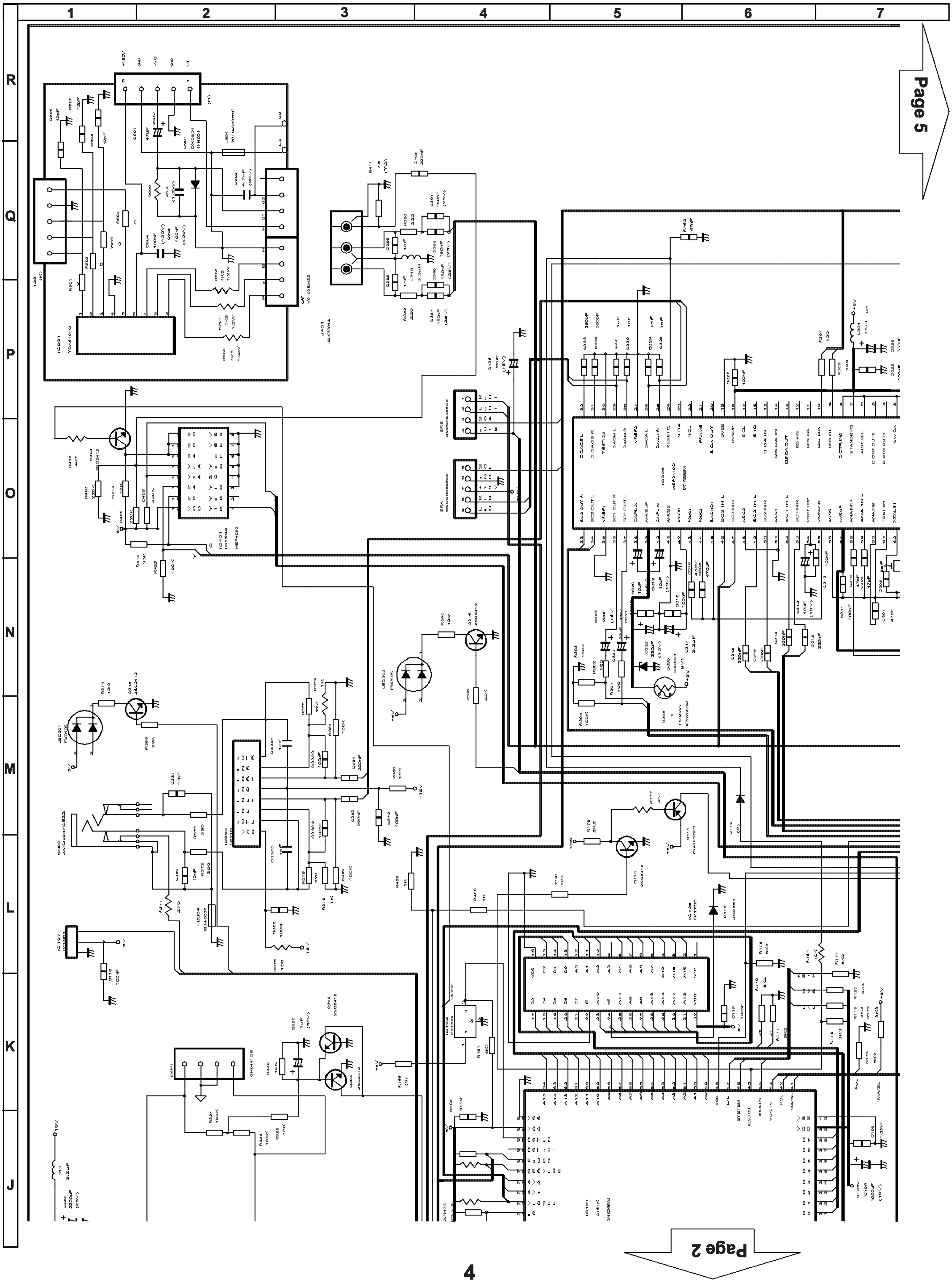
59DS-05H
66DS-05H
66ES-05H

SCHEMATIC DIAGRAM.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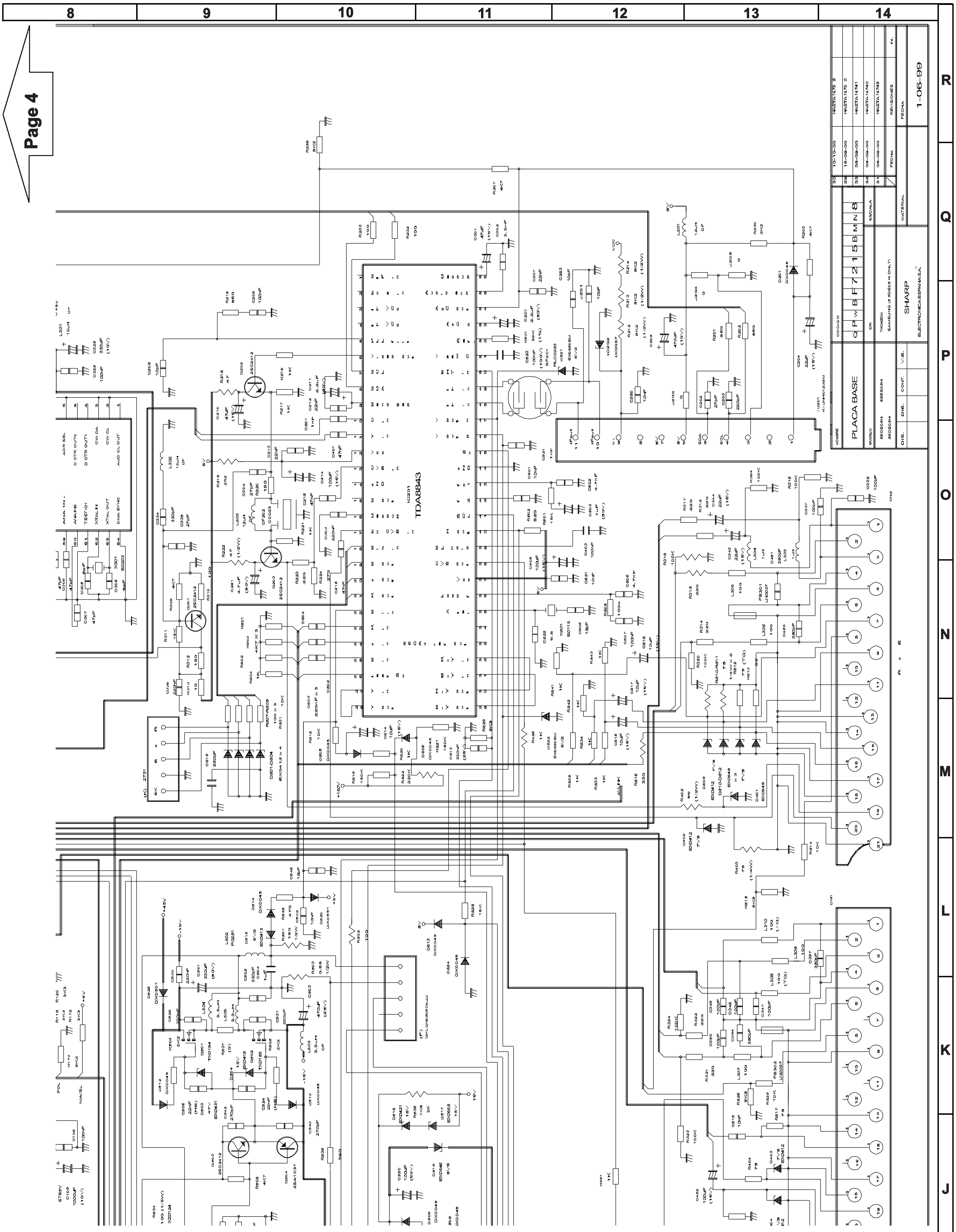
59DS-05H
66DS-05H
66ES-05H

SCHEMATIC DIAGRAM.

Page 4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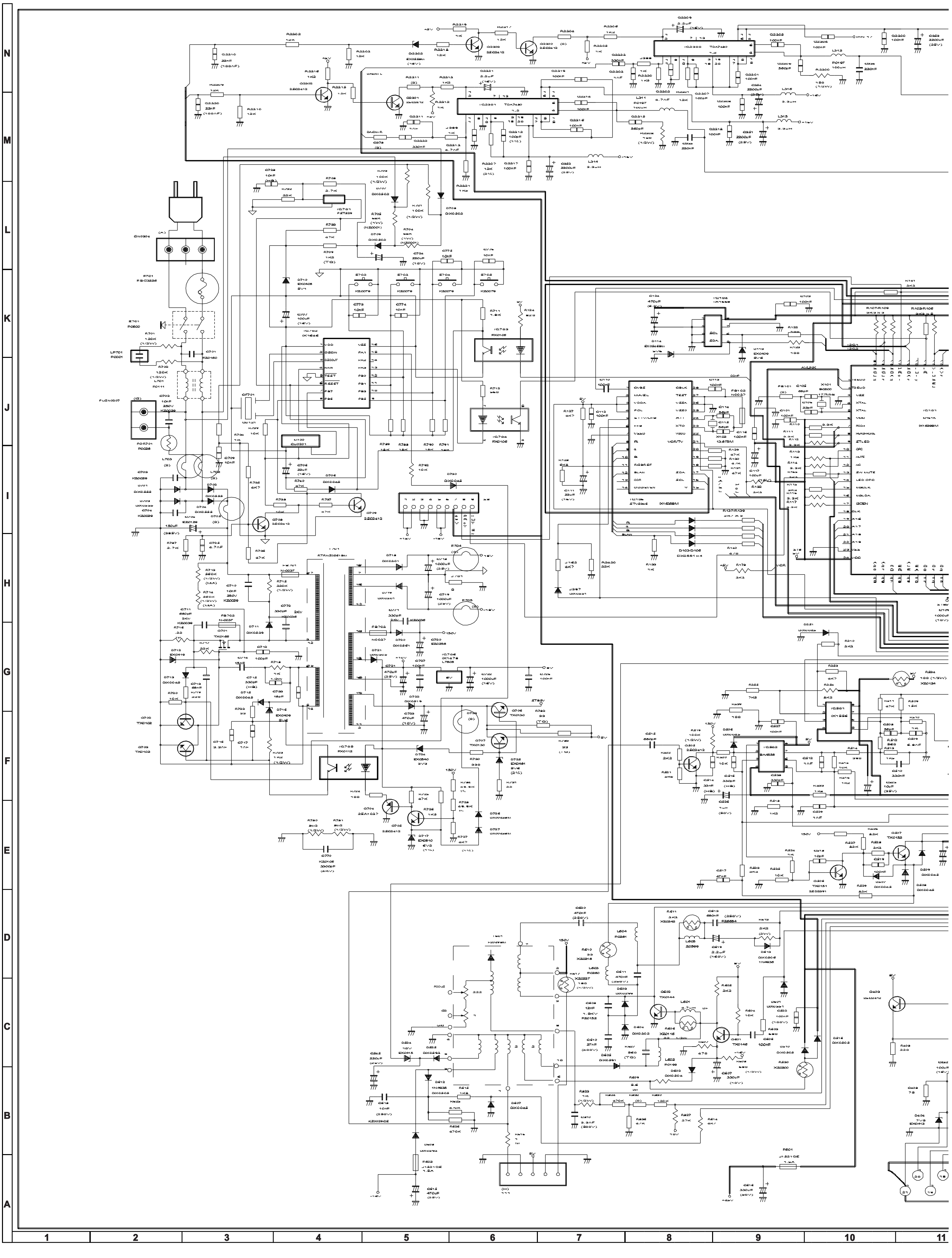
IC201
TDA8843
PLACA BASE
SHARP
ELECTRONICA ESPAÑA S.A.
1-06-99

Page 3

SCHEMATIC DIAGRAM.



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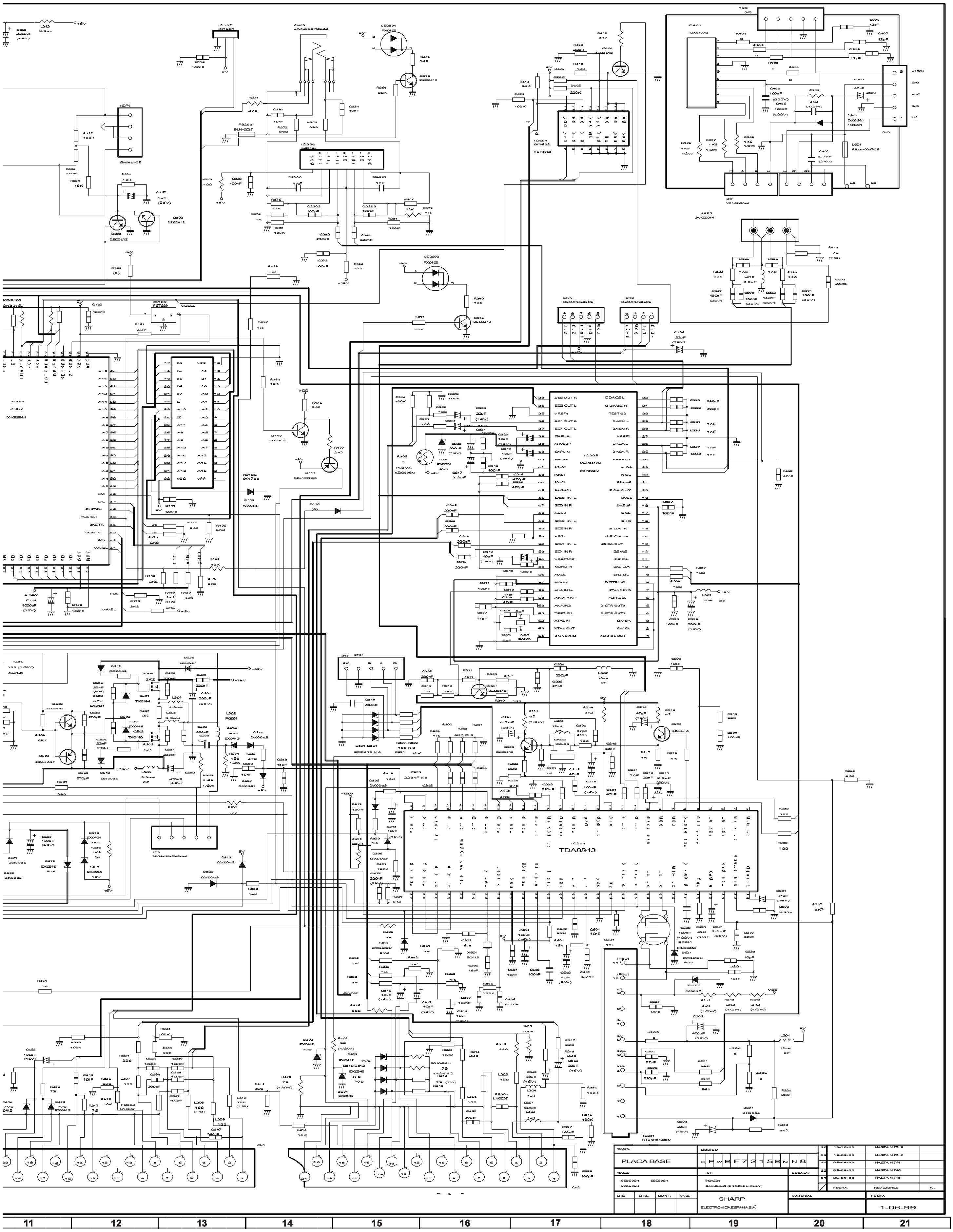
TDA8843
IC305
IC201
IC907
TU201
RTUNH0129BM
PLACA BASE
CODIGO
QPWBF7215BMN8
MODELO
66DS05H 66ES05H
59DS05H
CRT
THOMSON
SAMSUNG (59DS05H ONLY)
ESCALA
DIS.
DIB.
CONT.
V.B.
SHARP
ELECTRONICA ESPAÑA S.A.
MATERIAL
FECHA
1-06-99
HASTA N.75 9
HASTA N.75 0
HASTA N.741
HASTA N.740
HASTA N.746
FECHA
REVISIONES
N.
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21

SHARP ELECTRONICS (UK) LIMITED

CA1/CA10 Chassis Course Notes

Produced by

Sharp Electronics (UK) Limited
CE Technical Support
Sharp House
Thorp Road
Newton Heath
Manchester
M40 5BE

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Introduction to the CA10 Chassis

As with the last Sharp colour television chassis (CS) the new CA10 design incorporates the latest technology from Japan and Spain where the receivers are designed and manufactured at the production plant in Barcelona.

Once again the reliable switched mode power supply, based around a field effect transistor, is used to provide power for the operation of the set. This has changed little since the CS chassis, but a detailed explanation of its circuit operation is given in the following pages.

Extensive use is made of dedicated integrated circuits and the number of surface mounted IC's is kept to a minimum to maintain an easier level of serviceability. The majority of IC packages are of the dual in line type. A break down of the major IC's explaining their basic functions is outlined below.

IC101 is the only large surface mounted IC and provides overall system control.

IC104 stores all the user information such as tuning and picture settings as well as geometry and CRT drive characteristics. This is an eight pin surface mounted device

IC105 is the EPROM, which contains the program to run the main system microprocessor.

IC106 (STV5346) is a single chip teletext decoder/processor whose output is at RGB levels. This is a 28 pin surface mounted device.

IC201 (TDA8844) provides the time base generators (line and frame), IF stage, majority of the Y/C processing and video switching (including RGB).

IC304 (M5218L) is the headphone amplifier.

IC305 (MSP3410D) provides all the audio signal processing requirements, including decoding, volume control and signal switching.

IC401 (HEF4053) provides for video switching (including the Y and C signals).

IC702 provides primary power supply on/off control and communication with the main system processor for key scan and remote control functions. It also controls the receivers self timer operation.

IC901 (TDA6107Q) drives the CRT.

Note that IC101 and IC702 are produced by Sharp and therefore can only be obtained through the Sharp Spare Parts Centre. IC104 and IC105 are generally available, but contain programs and therefore must also be obtained direct from Sharp Spare Parts Centre.

As the tuner is directly controlled by the I^2C bus it enables direct channel entry and stable control of the tuning and AFT functions. By receiving controlling inputs from IC201 (IF processor) and IC106 (teletext processor) the main system processor can carry out automatic tuning and sorting.

Various audio inputs can be used to generate either mono, stereo or SRS (Sound Retrieval System) sound, depending on receiver specification - see next page for model specifications. Output from the top of the range receiver is 2 x 20W (MPO) and an additional 20W from the external sub-woofer. As the audio signal is controlled by the data bus, it is possible to have separate control of both loudspeaker and headphone outputs.

Video switching from a number of sources is possible, this includes RGB from a rear SCART socket and S-VHS from the rear AV SCART socket.

All of the above contribute to make a reliable and easily repairable television chassis, that is fitted into all of the new Sharp range of large screen television receivers as listed on the following page.

CA10 Receiver Specifications

The table below lists all of the current range (as of January 1998) of Sharp television receivers utilising the CA10 chassis. Note that the receivers featuring a sub-woofer will have an extra drive PWB fitted and the SRS models will have the SRS sound processing sub PWB fitted.

Features	51DS02H	51DS03H	51DS05H	59DS03H	59DS05H	66DS03H	66DS05H
Tube Size (inches)	21	21	21	25	25	28	28
Visible Screen (cm)	51	51	51	59	59	66	66
Tube Type	B Matrix	B Matrix	B Matrix	B Matrix	B Matrix	B Matrix	B Matrix
Number of Pre-sets	99	99	99	99	99	99	99
Auto Sort	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast Text	Yes	Yes	Yes	Yes	Yes	Yes	Yes
NICAM	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SRS/3D Sound	-	-	Yes	-	Yes	-	Yes
AI-OPC	-	-	Yes	-	Yes	-	Yes
On/Off Timer	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Rear S-VHS Input	-	-	Yes	-	Yes	-	Yes
21 Pin Euroscart	2	2	2	2	2	2	2
Ext Speaker Output	-	-	-	-	S Woof	-	S Woof
Power Output (MPO)	2x4	2x10	2x10	2x10	2x10+20	2x10	2x10+20
Headphone Jack	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Stand	Yes	Yes	Yes	Yes	-	Yes	-
Cabinet	-	-	-	-	Yes	-	Yes
Width (mm)	539	612	612	695	695	740	740
Height (mm)	468	458	458	537	537	566	566
Depth (mm)	484	492	492	431	431	470	470
S/B Power	3W	3W	3W	3W	3W	3W	3W

Note :

Sharp reserve the right to make design and specification changes for product improvement.

The performance specification figures are nominal values of production units. There may be some deviation from these figures in individual units.

To complete this range of television receivers, the CS chassis is used for the Dolby Pro-logic models 59CSD8H and 66CSD8H.

CA10 Block Diagram

To give an overview of the CA10 Chassis, the block diagram shown below represents a pictorial view of the receiver and its individual components.

16

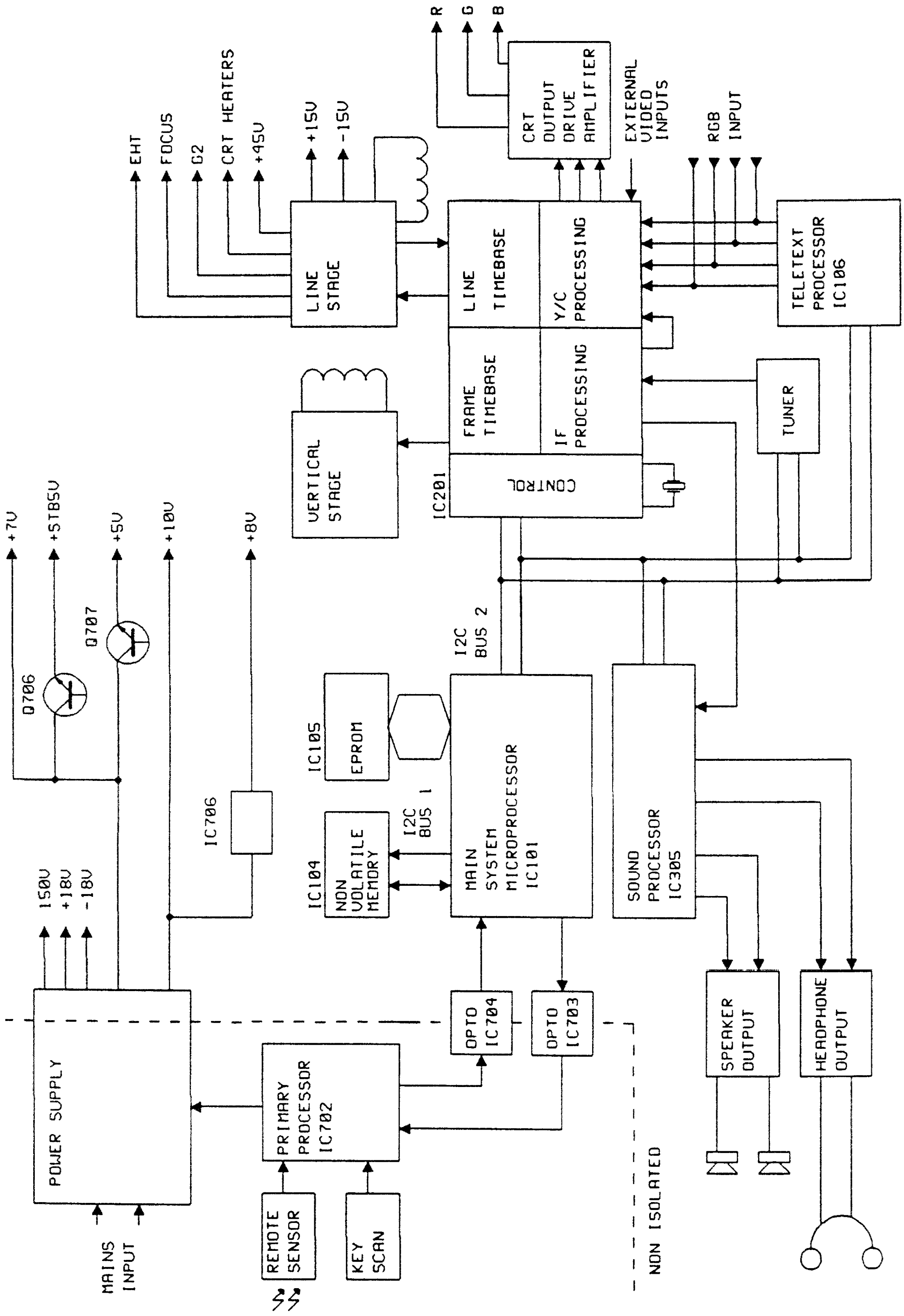
EHT
FOCUS
G2
CRT HEATERS
+45V
+15V
-15V
R
G
B
CRT OUTPUT DRIVE AMPLIFIER
EXTERNAL VIDEO INPUTS
RGB INPUT
LINE STAGE
LINE TIMEBASE
Y/C PROCESSING
TELETEXT PROCESSOR IC106
FRAME TIMEBASE
IF PROCESSING
TUNER
VERTICAL STAGE
IC201
CONTROL
+7V
+5TBSV
+5V
+10V
+8V
Q706
Q707
I2C BUS 2
IC105 EPROM
IC706
I2C BUS 1
IC104 NON VOLATILE MEMORY
MAIN SYSTEM MICROPROCESSOR IC101
SOUND PROCESSOR IC305
150V
+18V
-18V
POWER SUPPLY
PRIMARY PROCESSOR IC702
OPTO IC704
OPTO IC703
SPEAKER OUTPUT
HEADPHONE OUTPUT
NON ISOLATED
REMOTE SENSOR
KEY SCAN
MAINS INPUT

Figure 1 : Overall Block Diagram of the CA10 Chassis

Power Supply

This self running switched mode power supply is based around a single field effect transistor, Q701 and generates the following supplies for use in various parts of the receiver. Note that other supplies are generated by the line stage and are covered in the **Line Stage** section of these notes.

Supply	Purpose	Point of Generation
+18V	Audio and frame output amplifiers	D718, pin 8 of T701
-18V	Audio and frame output amplifiers	D719, pin 8 of T701
+150V	Line output, CRT drive amplifier and VT line generation	D720, Pin 4 of T701
+13V	Source of +8V supply	D711, pin 5of T701
+8V	IC201 supply	IC706
+7V	Source of STB5V and 5V	D722, pin 1 of T701
STB5V	Supply for IC101/2/5/6	Q706
+5V	Supply for IC305, tuner	Q707

Note : The voltages attributed to the rails on the circuit are not necessarily the measured voltage. See the **Power supply voltage line resistances to earth** section of these notes for actual measured voltages and nominal cold resistances to ground.

Mains input circuit

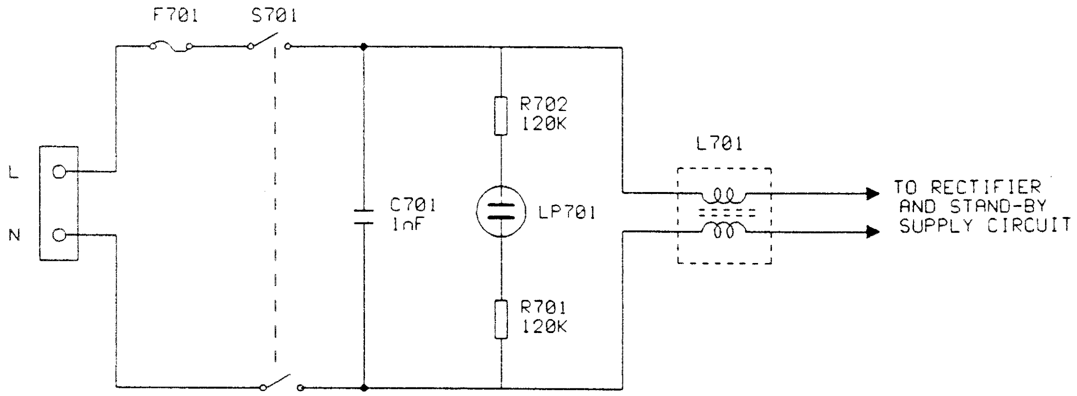

Figure 2 : Mains Filter and Indicator Circuit

From the mains plug (fitted with a 3A fuse), the mains passes into the set via connector GN0304 and into the fuse, F701 (3.15A anti-surge). After the mains switch, S701, the mains applied indication neon is connected across the live and neutral lines via R701 and R702. From this point the mains is fed to the de-gauss circuit, via L701 and the positor POR701, undesirable spikes generated by the de-gause operation, are removed by C702. Choke L701 provides further noise suppression. After L701 the mains is also sent to the standby control circuit. Finally, after passing through L702 and L703, the mains is supplied to the bridge rectifier.

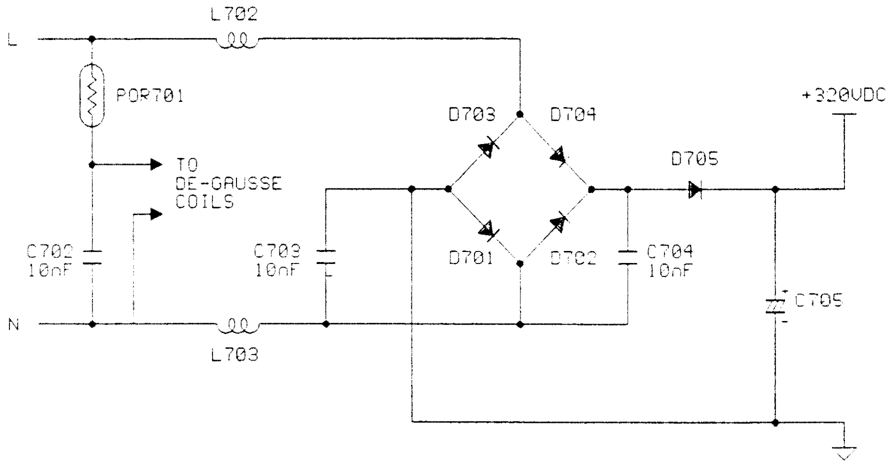

Figure 3 : Mains Rectifier Circuit

D701, D702, D703 and D704 full wave rectify the incoming mains and this rectified voltage is smoothed by C705. The resultant 320VDC is now fed to the switched mode power supply.

D705 is used to limit possible damage caused to the bridge rectifier from internally generated noise that could come close to the PIV of the diodes. Note that in some versions of the CA10 chassis, this diode is not fitted.

Standby operation

Because of proposed legislation, which will limit the stand by power consumption, changes have been made to the operation of the set during the stand by mode. This is achieved by muting the operation of the power supply in the standby mode so that no oscillation takes place. The operation of the power supply described below, therefore, relates to when the set is running. How the set comes out of standby will be covered in the **Power on control** section of these notes.

Start up operation

Rectified and smoothed mains voltage (+320VDC) is used to provide the start up voltage to the gate of Q701. Current flows via R713 and R714 causing C714 to charge up, the earth return for the capacitor is via R718 and winding 15/14 of T701. This allows a voltage to be built up on the gate of Q701 (this will turn on Q701 when it gets to about four and a half volts). D712 ensures that the steady DC on the gate of Q701 does not exceed twelve volts as any voltage higher than this may damage the device. C712 removes any high frequency pulses that may damage Q701.

As Q701 turns on, current will flow via the bridge rectifier, pins 17 and 12 of T701 and the source/drain of Q701 finally returning to the bridge rectifier by the earth return resistor, R716. This will induce an emf into the primary winding of the chopper transformer, which will be reflected by the secondaries via the magnetic induction within the transformer itself.

The voltage generated by the winding connected between pins 14 and 15 will also increase as the conduction of Q701 increases. This increase in voltage will cause D716 to conduct when its zener voltage is reached (5.6 volts). Therefore C713 will start to charge and when the base/emitter voltage of Q703 reaches 0.65 volts it will conduct and effectively remove the gate supply. Q701 is now turned off and current ceases to flow in the primary winding of T701 and the emf will start to decay.

As the secondary voltages decay, pin 15 of T701 will go negative and this negative charge is transferred via C714 to the gate of Q701, holding the FET fully off for a time period decided by the charging rate of C714 (via R713/4) and the discharge rate of C713 (via the base/emitter junction of Q703). Once the magnetic field has collapsed totally, the cycle is repeated.

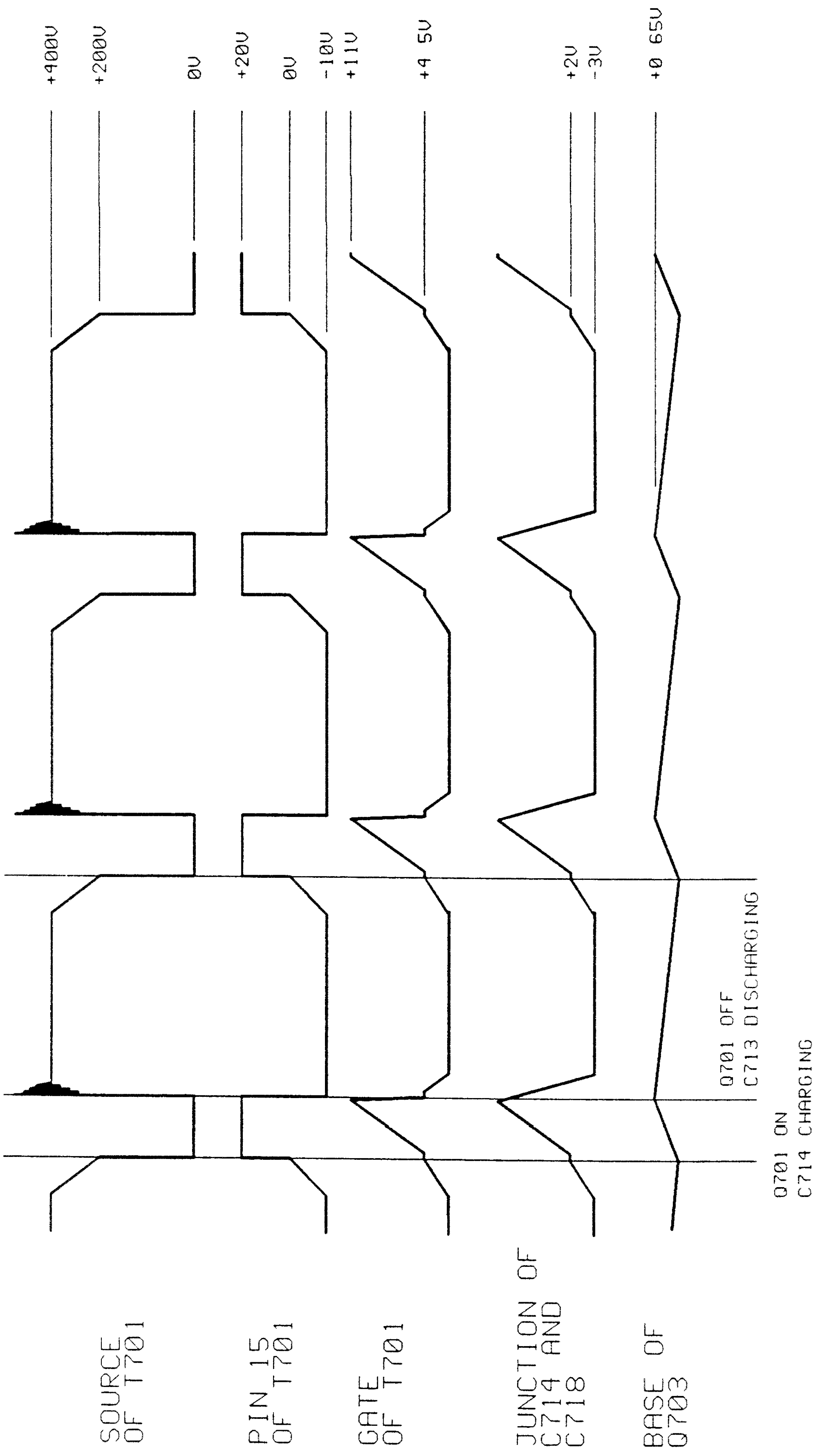
+400V
+200V
0V
+20V
0V
-10V
+11V
+4.5V
+2V
-3V
+0.65V
SOURCE OF T701
PIN 15 OF T701
GATE OF T701
JUNCTION OF C714 AND C718
BASE OF Q703
Q701 OFF
C713 DISCHARGING
Q701 ON
C714 CHARGING

Figure 4 : Power Supply Waveforms

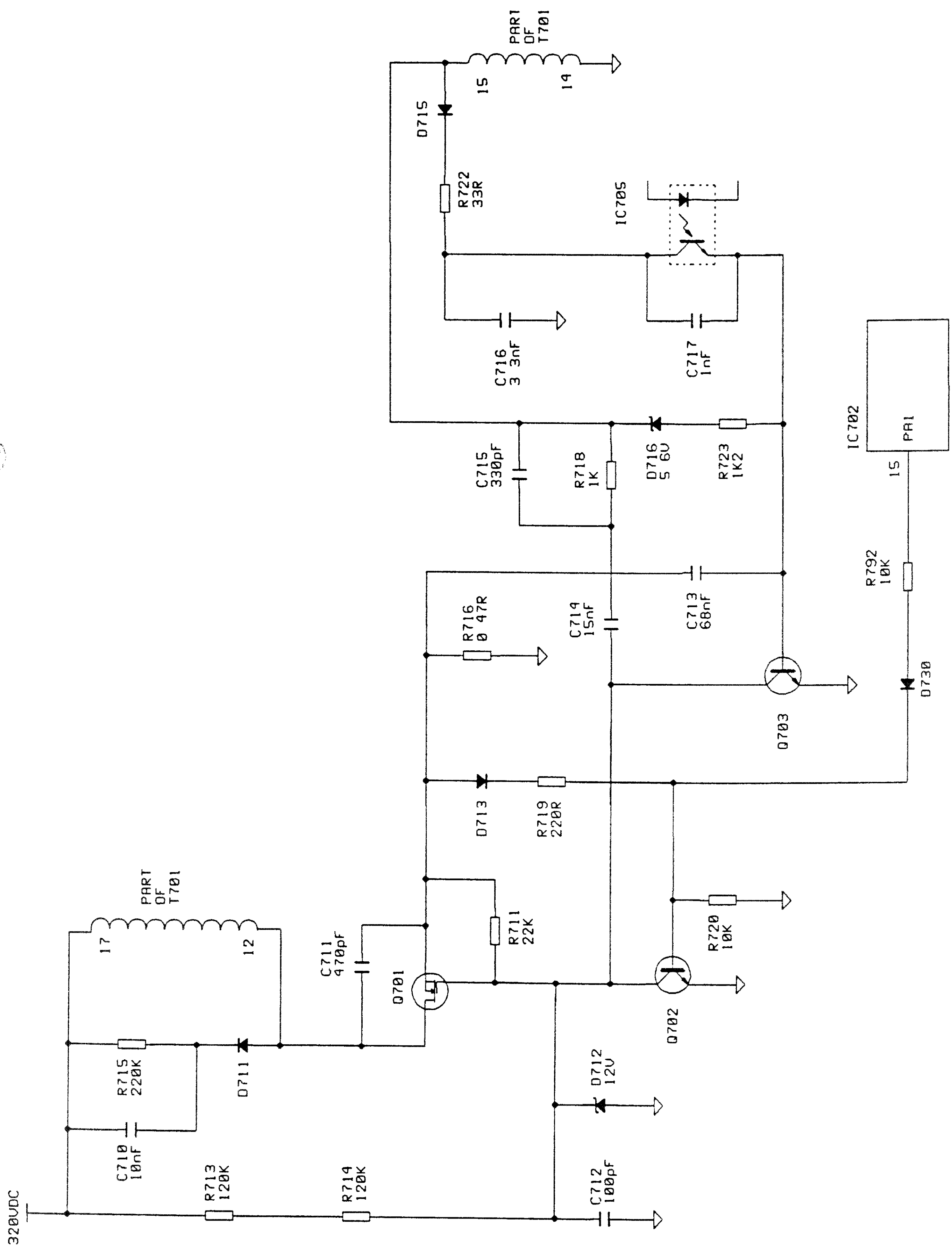
PART OF T701
15
14
D715
R722 33R
IC705
C716 3 3nF
C717 1nF
IC702
PR1
15
C715 330pF
R718 1K
D716 5 6V
R723 1K2
R792 10K
R716 0 47R
C714 15nF
C713 68nF
D730
Q703
D713
R719 220R
PART OF T701
17
12
C711 470pF
R711 22K
Q701
R720 10K
Q702
D712 12V
R715 220K
D711
C710 10nF
R713 120K
R714 120K
C712 100pF
320VDC

Figure 5 : CA10 Power Supply - Non-isolated Side

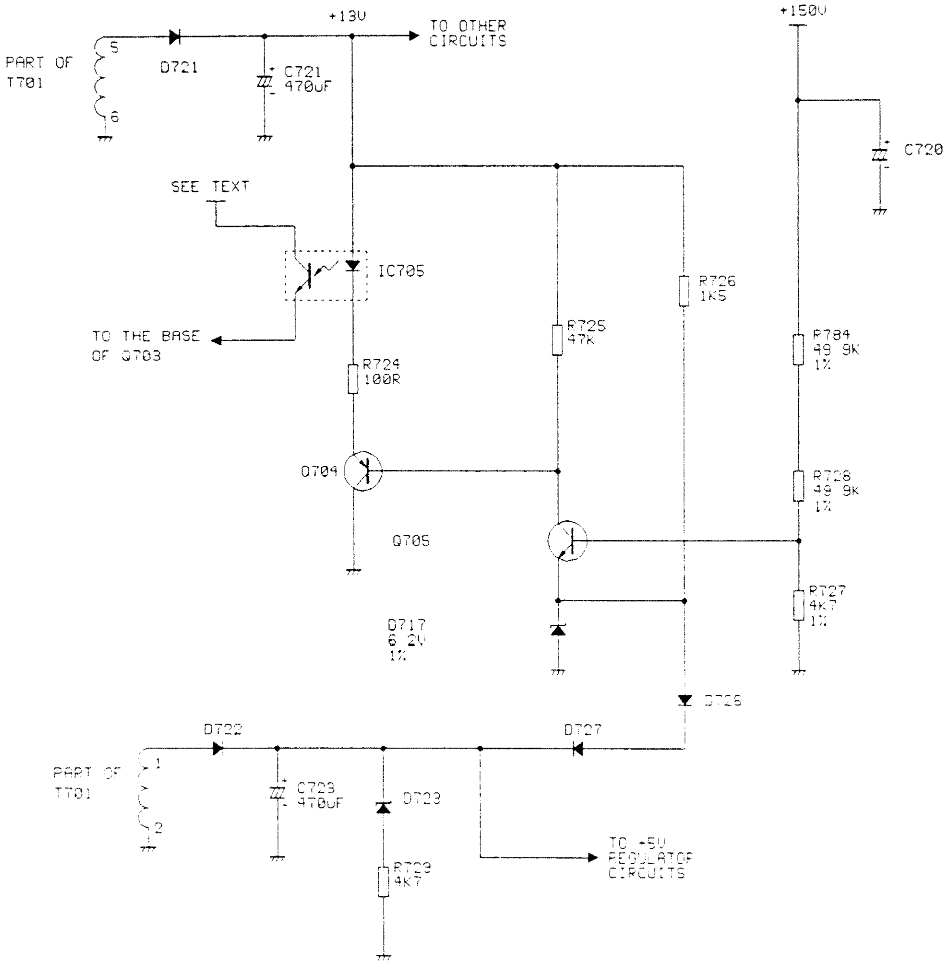
+13V
TO OTHER CIRCUITS
+150V
PART OF T701
5
6
D721
C721 470uF
C720
SEE TEXT
IC705
TO THE BASE OF Q703
R726 1K5
R725 47K
R784 49 9K 1%
R724 100R
Q704
R728 49 9K 1%
Q705
R727 4K7 1%
D717 6 2V 1%
D726
D722
D727
PART OF T701
1
2
C723 470uF
D723
R729 4K7
TO +5V REGULATOR CIRCUITS

Figure 6 : Power Supply Regulation Circuit - Secondary Side

Voltage regulation

Voltage regulation is provided by the feed back through the opto coupler, IC705. The 150 volt line is used as the controlling source and a reference is provided from the +13V supply. Protection is also incorporated via the +7V supply for faults that may occur on either of the five volt supplies (STB5V and +5V).

Current flowing through the opto coupler LED will effect its brightness and therefore the conduction of the light sensitive transistor. This will control the time taken to charge C713 from the supply generated by D715 and R722 and therefore will control the turn on time of Q703, note that the earth return for C713 is via R716.

As the collector of Q703 is connected to C714 this action will in turn affect its charging time and the on/off time of Q701. As the charge/discharge of C714 is controlled by the switching of Q701 its base capacitor, C713, is the timing control influence. As the discharge of C713 is constant, the off time will remain at approximately the same period during each cycle, because its discharge path remains the same through R716. Whereas the charging of C714 will control the on time, i.e. when its charge is above the threshold turn on voltage on Q701 or +4.5V. Therefore it can be noted that an increase in load will slow down the frequency of operation.

Note that D715, R722 and C716, on the primary side of the opto coupler, provide a voltage supply circuit to the collector of the transistor contained within IC705. Also note that on the secondary side of the regulation circuit, the supply for the reference zener diode, D717 is taken from the +13V supply.

Supply increase

If the 150 volt supply line were to increase, the voltage on the base of Q705 would also increase. As the emitter of Q705 is held steady by the zener diode D717, at 6.2V, the collector will start to drop. This will allow Q704 to conduct more and the LED will become brighter.

As the LED becomes brighter, the transistor within IC705 will conduct more allowing C713 to charge faster and thus turning on Q703 quicker. Q703 will discharge Q714 and turn Q701 off, making the on time of Q701 shorter. The emf will decrease and the voltages induced in the secondary windings of T701 will also decrease.

Supply decrease

If the 150 volt supply line were to decrease, the voltage on the base of Q705 would decrease. As the emitter of Q705 is held steady by the zener diode D717, at 6.2V, the collector will start to rise. Q704 will conduct less and the LED will become less bright.

As the LED becomes less bright, the transistor within IC705 will conduct less giving a lower voltage on the base of Q703 and C713 will charge more slowly. Q703 will now turn on later in the cycle and allow C714 to charge up for longer. This will turn on Q701 for longer and the current through the primary winding (12 and 17) of T701 will increase. The emf will increase and the voltages induced in the secondary windings of T701 will also increase.

Note

The voltage present at the junction of R784/R728 and R727 will be exactly 6.7464V when the supply is 150V. As the emitter of Q705 is held at 6.2V by the action of zener diode, D717, the collector will follow the base voltage. As the h_{fe} of Q705 (2SC2412) is high it will amplify the voltage on its base so that the voltage swing on its collector will be great enough to vary the base voltage of Q704 dramatically. Q704 is effectively a current amplifier which allows the LED inside the OPTO coupler to be driven through its range of intensity.

C720 ensures that no short time constant variables effect the operation of the regulation circuit. If the regulation were to change too quickly, there may be a chance that the power supply will oscillate at a high frequency - this is undesirable.

As the tolerances in this part of the circuit are high and impedances are also relatively high, there is a risk of circuit malfunction if a voltmeter with too low an impedance is used. In worst case this could lead to failure of the power supply. It is recommended that if fault finding has to be carried out in this part of the circuit, then an oscilloscope is used.

Protection

Protection is provided should one of the five volt supplies, STB5V and +5V, drop to an unacceptable level. This is achieved by monitoring the +7V supply which is used to generate the STB5V and +5V lines.

Should the +7 volt supply drop to a point whereby diodes D726 and D727 start to conduct, the voltage on the emitter of Q705 will drop. This will cause the collector of Q705 to drop, turning Q704 on harder, making the LED brighter and turning on Q703 sooner, dramatically decreasing the discharge time of C714 and thus the ON time of Q701. Therefore reducing the current flowing in the primary winding of T701.

When the current flowing in the primary winding of T701 decreases, so will the secondary voltages. This will cause the voltage generated by D722 (+7V rectifier) to also drop. This will reinforce the above action and the power supply will attempt to shut down. During this cycle, there will come a point where it becomes impossible to maintain the conduction of Q703 (as the charge on C713 decays to below +0.65V) and the power supply will start up again. If the condition of the +7V (low supply) line continues the set will continually trip.

Over current control

Over current control is performed by monitoring the amount of current passing though the chopper output transistor drain earth return resistor, R716. This resistor is an extremely low value, 0.47R, and Ohms Law dictates that the current flowing through it must be proportional to the voltage across it. If the base voltage required to turn on Q702 is +0.65V then the voltage across R716 to 'trip' the circuit would have to be approximately 1.2V (if the volt drop across D713 was 0.6V). This results in a trip current through R716 of 2.55A.

The voltage developed across R716 is used to turn Q702 on via D713 and potential divider, R719/20. If Q702 turns on it will discharge C714 rapidly removing the gate bias and Q701 which will turn off until the current trough R716 decreases to a point where Q702 turns off and Q701 turns on again (after C714 has charged up to four an a half volts). In the case of heavy current over load this will cause the power supply to whistle as the frequency of the power supply stopping and starting will be within the audio range.

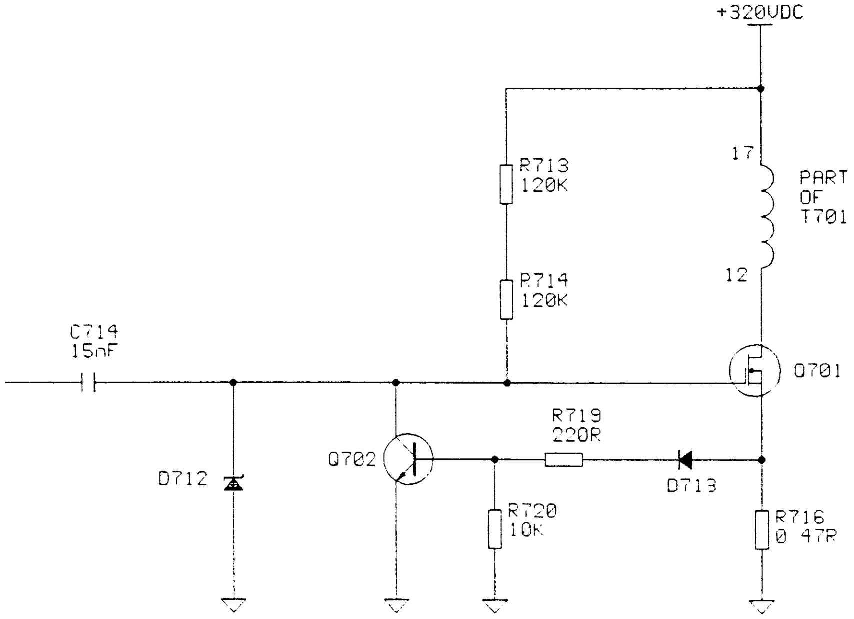
+320VDC
R713
120K
17
PART
OF
T701
12
R714
120K
C714
15nF
Q701
R719
220R
Q702
D712
D713
R720
10K
R716
0 47R

Figure 7 : Current Regulation Circuit

D713 is used to set the voltage / current (through R716) at which Q702 will initiate an "over current" action. Therefore, the smaller screen sizes fitted with the CA10 chassis may not have this diode in the circuit shown above

Snubber circuit

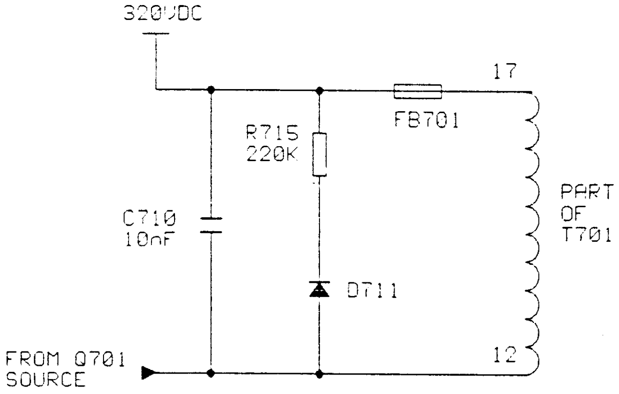
320VDC
17
FB701
R715
220K
PART
OF
T701
C710
10nF
D711
12
FROM Q701
SOURCE

Figure 8 : Snubber Circuit

When the magnetic field within T701 collapses, the back emf generated across the primary winding causes large voltage spikes to appear across pins 12 and 17. If these spikes are not suppressed, then damage will occur to the primary side of the power supply.

To prevent this from happening a snubber circuit, consisting of D711, R715 and C710 is used. Thus when pin 12 becomes positive with respect to pin 17, D711 will conduct and current will flow through R715. The spike will be damped by the action of C710 and R715. FB701 removes any HF noise.

Power on control

Primary processor power supply

As the chopper supply stage is shut down during the standby mode, it is necessary to provide power to the control circuitry from another source. This is achieved by supplying the mains voltage to a shunt regulator circuit as shown in the diagram below.

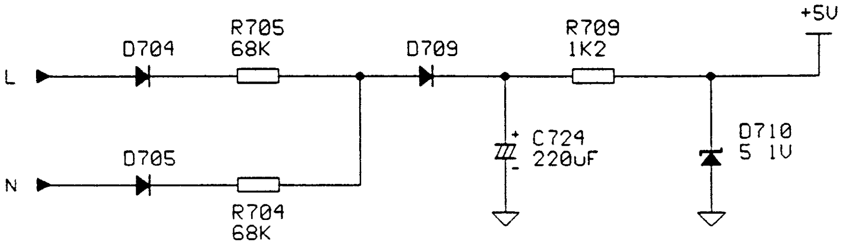

Figure 9 : Primary Processor Power Supply

This simple circuit provides a positive five volt supply to the reset IC, IC701 and microprocessor, IC702.

Power supply turn on

At mains application, the primary microprocessors reset IC, IC701, will provide a positive going reset pulse to initialise IC702. At the same time the ceramic filter, CF701 will start to oscillate. This sequence of events will initialise IC702, the key scan and remote control function will become operational.

When pin 15 (PA1) of IC702 goes low, either by pressing one of the four buttons on the front of the television or by use of the remote control, the base bias to Q702 will be removed and it will turn off, its collector voltage will therefore rise. The power supply will now start up in line with the description given previously.

If pin 15 (PA1) of IC702 goes high, it will turn on Q702 via R792 and D730. This action will remove the voltage on the gate of Q701 and turns it off. As this condition is permanent (for the period of time that pin 15 is at five volts), the power supply will turn off until a new power on command is issued by IC701..

Communication is maintained with the system microprocessor, IC101, via the two opto couplers. IC704 is used to send data from IC702 to IC101 for control purposes - button pressing and remote control. IC703 is used to control IC702 from IC101, i.e. to shut down the set if a protection fault occurs. Note that the reset pin of IC701 is also connected to this opto coupler via D706, so that if the transistor conducts heavily, pin 6 of IC702 will go low. IC702 will now turn the power supply off which will remove the supply to the main processor and IC703 will stop conducting therefore pin 6 will be allowed to rise, resetting IC702 and in turn powering up the supply again. Note that the supply to IC702 is always there.

Primary Processor

As described previously, to control the operation of the set in the standby mode a primary processor is utilised. The circuit diagram of this part of the circuit is shown below.

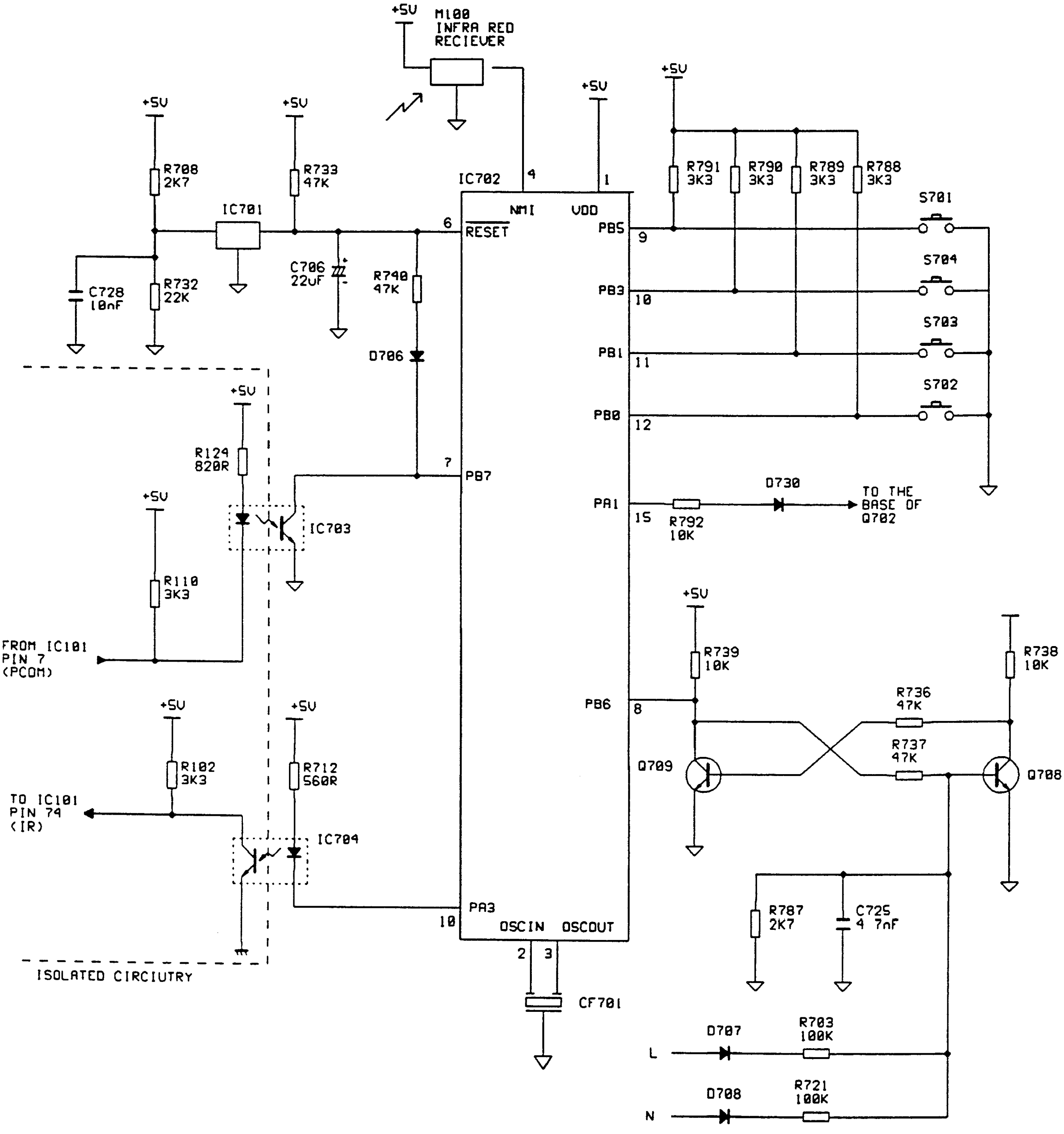
+5V
M100
INFRA RED
RECIEVER
+5V
+5V
R708
2K7
R733
47K
IC701
C706
22uF
R740
47K
C728
10nF
R732
22K
D706
IC702
4
1
NMI
VDD
6
RESET
PB5
9
PB3
10
PB1
11
PB0
12
7
PB7
PA1
15
PB6
8
PA3
10
OSCIN
OSCOUT
2
3
CF701
+5V
R791
3K3
R790
3K3
R789
3K3
R788
3K3
S701
S704
S703
S702
D730
R792
10K
TO THE
BASE OF
Q702
+5V
R124
820R
IC703
+5V
R110
3K3
FROM IC101
PIN 7
(PCOM)
+5V
R102
3K3
+5V
R712
560R
TO IC101
PIN 74
(IR)
IC704
ISOLATED CIRCIUTRY
+5V
R739
10K
R738
10K
R736
47K
R737
47K
Q709
Q708
R707
2K7
C725
4 7nF
D707
R703
100K
L
D708
R721
100K
N

Figure 10 : Primary Side Microprocessor

The two transistors Q708 and Q709 comprise a monostable, which is triggered from the mains input at double frequency, i.e. 100Hz. The square wave signal on pin 8 (PB6) is used to control the on timer. This is necessary due to the fact that in standby, the main system microprocessor, IC101, is dormant, i.e. no supply and therefore can not perform any functions. The off timer function is controlled within IC101.

System Control

Resets and oscillators

When the power supply starts up the program within the main microprocessor needs to be reset. This is achieved with the use of the circuit shown below.

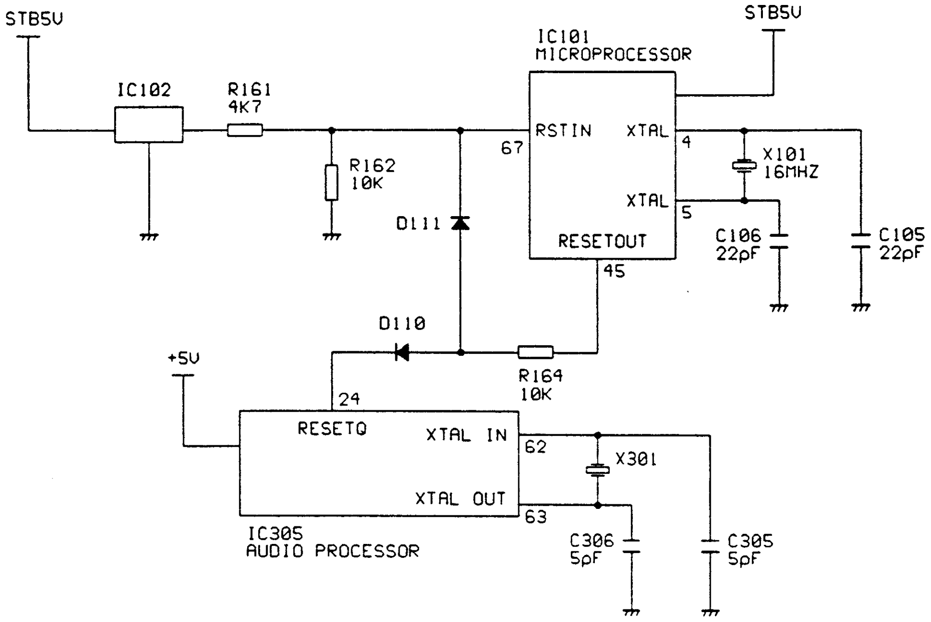
STB5V
IC102
R161
4K7
R162
10K
D111
D110
+5V
R164
10K
IC101
MICROPROCESSOR
RSTIN
XTAL
XTAL
RESETOUT
67
4
5
45
STB5V
X101
16MHZ
C106
22pF
C105
22pF
RESETQ
XTAL IN
XTAL OUT
24
62
63
IC305
AUDIO PROCESSOR
X301
C306
5pF
C305
5pF

Figure 11 : Reset Operation Circuit

When the STB5V supply has reached its correct level, the output from IC102 changes from a low to a high level to reset IC101 on pin 67 (RSTIN). After IC101 has reset itself it gives a further reset to the audio processing IC, IC305 via pin 45 (RESETOUT). This pin changes from low to high, then back to low and finally remains high as shown in the diagram below. IC305 is now reset.

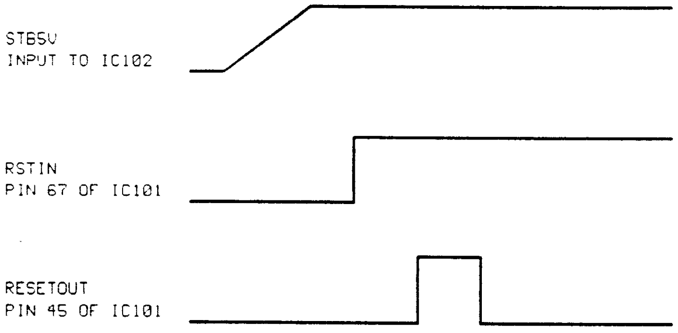
STB5V
INPUT TO IC102
RSTIN
PIN 67 OF IC101
RESETOUT
PIN 45 OF IC101

Figure 12 : Reset Pulse Timing

Once the main system microprocessor, IC101, has reset and the oscillator is running at the correct frequency the internal programme sequence is initiated. It first checks that the internal functions of the IC are working correctly then checks the devices connected to it via the I^{2}C bus. If any errors are encountered then the microprocessor will either shut down or produce a fault symptom - see the **I^{2}C bus line disconnection** part of these notes for more details.

When the microprocessor has satisfied itself that all devices connected to it are operating correctly, it will read information from the EEPROM, IC105, to operate the set in the right sequence.

Data communication

Within the CA10 chassis, there are a number of data control signals that pass to and from the main system microprocessor, IC101. There are two basic types, serial and parallel as shown in the diagram below.

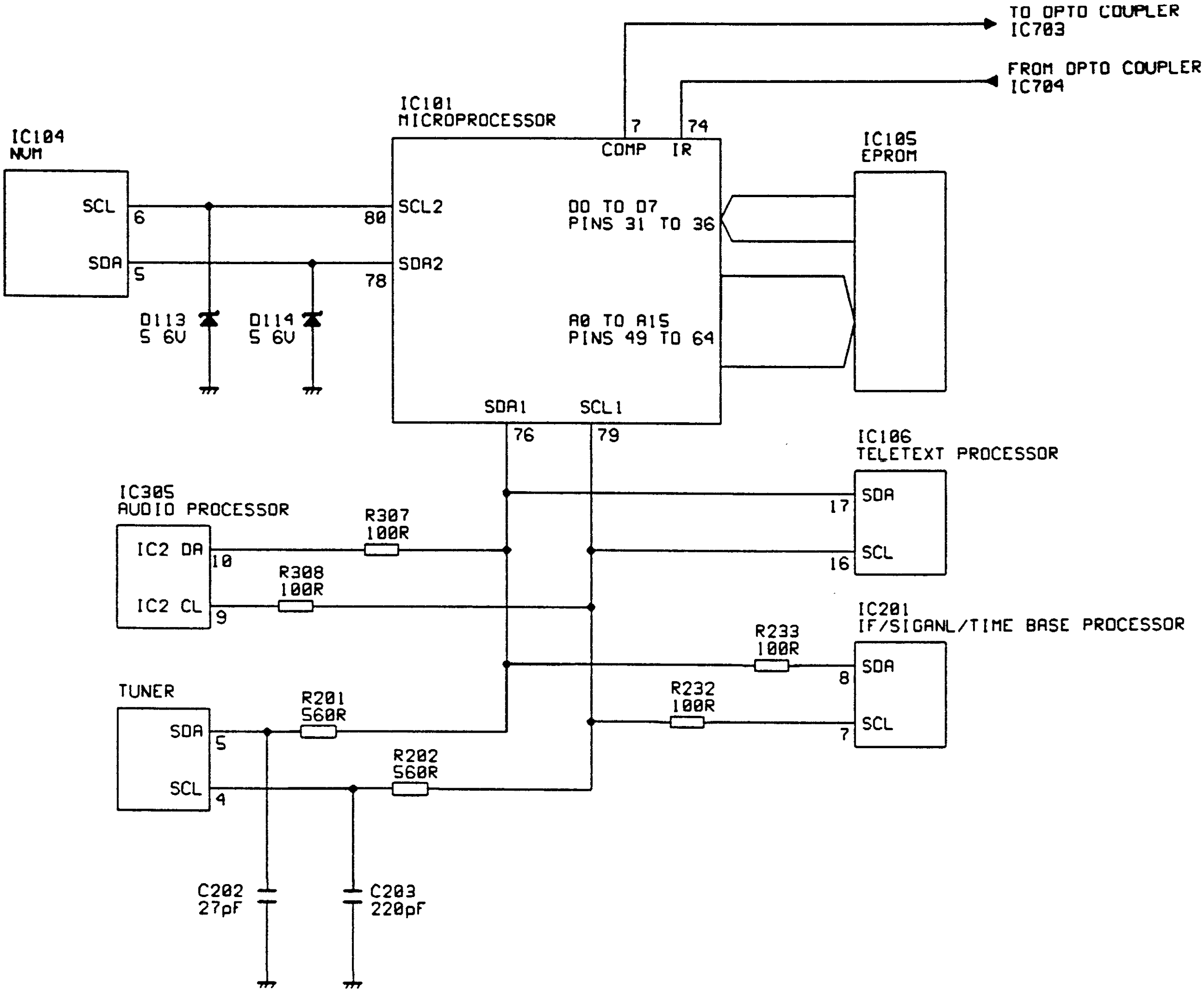
TO OPTO COUPLER
IC703
FROM OPTO COUPLER
IC704
IC101
MICROPROCESSOR
7
74
COMP
IR
IC104
NVM
SCL
SDA
6
5
80
78
SCL2
SDA2
D0 TO D7
PINS 31 TO 36
A0 TO A15
PINS 49 TO 64
IC105
EPROM
D113
5 6V
D114
5 6V
SDA1
SCL1
76
79
IC106
TELETEXT PROCESSOR
SDA
SCL
17
16
IC305
AUDIO PROCESSOR
IC2 DA
IC2 CL
10
9
R307
100R
R308
100R
IC201
IF/SIGNAL/TIME BASE PROCESSOR
R233
100R
8
7
R232
100R
TUNER
SDA
SCL
5
4
R201
560R
R202
560R
C202
27pF
C203
220pF

Figure 13 : Data Communication of IC101

I^2C bus

There are two I^2C buses used to communicate serial information to and from IC101. SDA1 and SCL1 is used to communicate with IC106 (Teletext processor), IC305 (Audio Processor), IC201 (IF, signal and time base processor) and the tuner. Each feed is current limited from the processor by the use of resistors (except for the teletext processor which is connected directly). Isolating these lines can be useful for fault finding - see the **I^2C bus line disconnection** section of these notes for more details.

The other I^2C bus is used for exclusive communication with the non volatile memory, IC104. IC104 contains all the user default values such as tuning information and picture control settings as well as geometry settings, grey scale information, chassis operating characteristics (text, NICAM etc). As this IC may be corrupted by glitches on the communication lines, D113 and D114 are used to suppress any spikes greater than 5.6 volts that may appear on the clock and data lines.

Parallel communication

Parallel communication exists between the EPROM and the microprocessor. The EPROM is where the main programme to run the various functions of the set are held eg Text programme, NICAM programme. As it is necessary for the processor to have fast access to this data, it is connected via a sixteen bit address line. The data is carried on an eight bit line.

Protection circuits

There is a protection input on IC101, pin 77 (PROT) which causes the set to shut down should there be a fault with the audio output stage.

When the audio output is operating correctly, the feed to the loudspeaker will have an average DC level of zero volts. If an imbalance were to occur whereby the signal became predominately more positive or negative, this could lead to failure of the audio output devices or loudspeaker. To alleviate this possible problem, the circuit shown below is used to turn off the set should the situation arise.

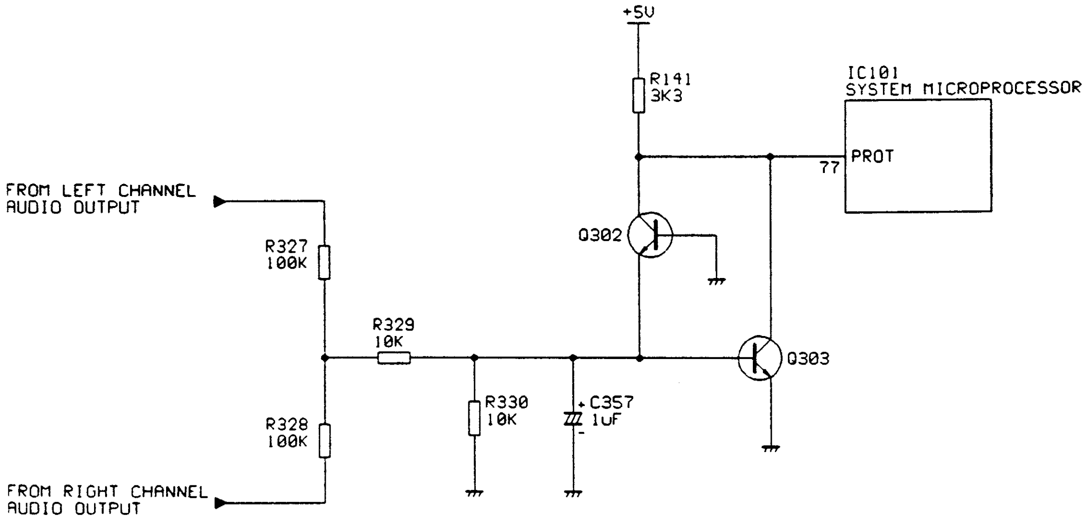

Figure 14 : Audio Protection Circuit

Under normal conditions, both Q302 and Q303 are turned off and the voltage present on pin 77 of IC101 is held high by the 3k3 pull up resistor R141. Should one of the outputs go more positive, then the DC level developed across C357 will increase. If this increase exceeds 0.6V, then Q303 will turn on, pulling down pin 77 and shutting down the set.

If one of the outputs were to go too negative, then the charge on C357 would drop, if this drop is greater that -0.6V then Q302 will conduct on pin 77 will be pulled low. Thus the set would shut down.

Software reset

As with the previous large screen chassis, the NVM is down loaded with its default information when the set is first powered up after manufacture. This means that whenever a NVM is ordered, it will be the same for all types of chassis (previous NVM's have come pre-programmed for the receiver in question).

If the information within the NVM is corrupted or settings/adjustments can not be made, then it is necessary to re-initialise the NVM. This is done using the following procedure.

1. Enter the service mode by pressing the channel down and volume up buttons on the front of the receiver, while turning on the mains power. Note that the two buttons have to be kept pressed until the receiver turns on.
2. Select the NVM position 00.
3. Set this location to 01.
4. Store the information by pressing the stand by button on the remote control.
5. Turn the set off at the mains.
6. Turn the receiver back on. It will take about thirty seconds for the receiver to start up as the microprocessor is down loading the information into the NVM.

Some settings may need sight adjustment as the preset values are based on no tolerance settings , in reality some will vary. Note that the above location of 00 is for the CS chassis type, to date this location for the CA chassis is unknown. Please consult your Technical Liaison Officer for more details.

Line Stage

Line signal generation is carried out within IC201, with synchronisation being supplied by the incoming sync pulse. The line stage generates various supplies, including EHT, focus, G2, A1 and heaters and the line scan coil drive signal.

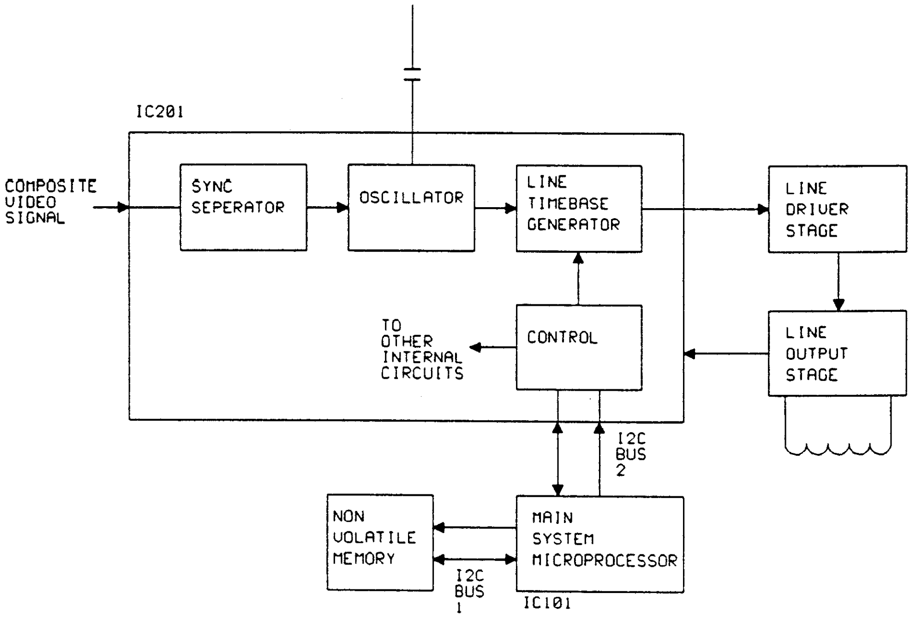

Figure 15 : Block Diagram of Line Stage

Line time base generation

IC201 generates the line drive signal internally using an oscillator whose frequency is controlled by various external components, the output of this oscillator is approximately 15.625kHz. Synchronisation is taken from the incoming video signal (tuner or video inputs) line synchronisation pulse when a signal is being received, in all other cases the oscillator is left to free run. When free running the on screen display is locked internally by comparing the sand castle pulse with the graphical information.

When the set is first turned on, using the standby button, the line oscillator runs at twice line speed - 31.25kHz. IC 201 then monitors the feed back from the line stage on pin 41 (SCL). When this signal is correct, the oscillator switches to 15.625kHz. The reason for this is so that the capacitors on the secondary windings of the line output transformer charge up faster to enable the line stage to reach its optimum operating characteristics quickly. This will prevent any excessive strain being put on the windings of the line output transformer. It is also necessary as the line drive circuit uses secondary supplies from T601 to ensure that the output transistor is turned hard on, if the line speed was not doubled then the set would not have enough energy to start up.

Line drive circuit description

The line drive circuit does not use a conventional coupling transformer, but is instead directly coupled to the drive IC as shown in the diagram on the next page.

From pin 40 of IC201 (H OUT) the line drive signal is fed through the DC blocking capacitor C606 into the base of Q601. D601 prevents any spikes that may appear on the drive signal from damaging the rest of the circuit. R604 pulls up the base of Q601 to the +13V supply.

As the line drive starts up at 31.25kHz, there will be no voltages generated by the line output stage to enable the line driver circuit to operate correctly. Therefore a feed is taken from the +13V and -16V lines off the chopper stage. In this situation, when Q601 is on the base of Q602 will be taken low (+13V plus -16V giving -3V) and Q602 will conduct. When its base goes low its collector voltage will start to rise, but this rise is limited by a number of factors. First is R605 and the second is the current drawn by Q602 itself.

Both of these conditions mean that the base of Q602 never exceeds 0.65V. As Q602 conducts an emf will be generated in the secondary winding of pins 4, 6 and 10.

Once IC201 has detected a feed back pulse, it will switch the line drive signal frequency to the correct running rate of 15.625kHz. At this point the supplies from the chopper stage are not used and those generated by the flyback transformer, T601, will take over.

As the current drawn by the base of Q602 is proportional to that drawn by its collector, it is desirable to have a low impedance source to drive its base (hence the use of a coupling transformer in a conventional line driver circuit). In this chassis a base current of four to five amps ins not unusual, and therefore a low impedance source need to be provided, which in this case is provided by the winding 4 to 10 of T601.

Assuming that the line has started up, when Q601 is off the current to turn on Q602 will flow from pin 10 of T601, through R605, L602 and L1/R606 into the base of Q602. This will turn on the device and current will flow in the primary winding of T601.

When Q601 is turned on, the current that would normally flow into the base of Q602 is now diverted through Q601's collector/emitter junction. This will turn off Q602 as its base voltage will drop below 0.65V. In actual fact the base voltage of Q602 drops to about -10V.

As can be seen from the diagram, pin 6 of T601 also generates the +45V supply used in the east/west correction circuit, but the voltage on the anode of D602 is negative. This is due to the fact that the waveform appearing at pin 6 is over 50V in the positive direction, but only about -15V in the negative direction (mainly overshoot). It is this negative going waveform that is rectified to produce the turn off voltage for Q602.

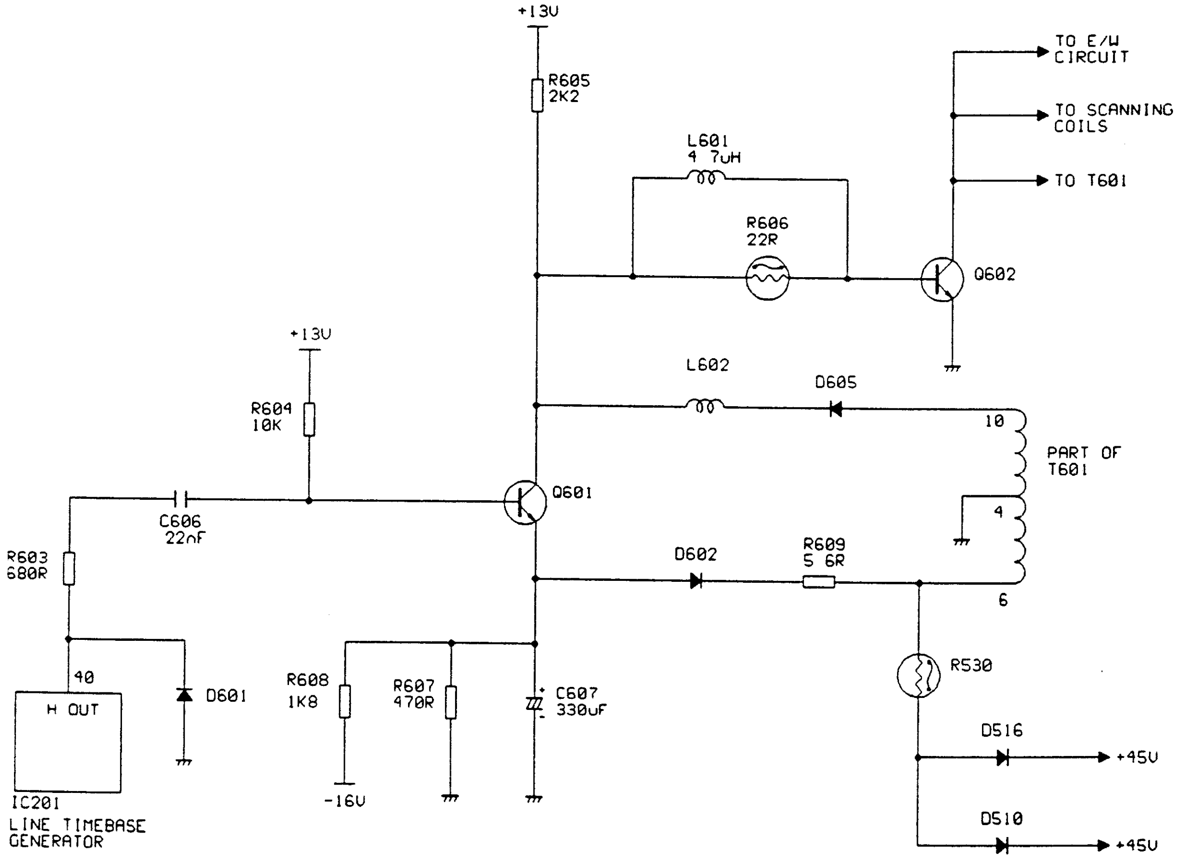
+13V
R605
2K2
TO E/W CIRCUIT
TO SCANNING COILS
TO T601
L601
4 7uH
R606
22R
Q602
+13V
L602
D605
10
PART OF T601
R604
10K
Q601
4
C606
22nF
R603
680R
D602
R609
5 6R
6
40
H OUT
D601
R608
1K8
R607
470R
C607
330uF
R530
D516
+45V
IC201
LINE TIMEBASE GENERATOR
-16V
D510
+45V

Figure 16 : Line Drive Circuit

R606 and L601 couple the line drive signal generated by Q601 to the base of the output transistor, Q602. These components are necessary to ensure that the transistor is fully saturated. They also, to some extent, provide protection to Q601 and IC201 should the output transistor go short circuit and allow excessive current and/or voltage to appear on its base.

Line output circuit description

To enable enough emf to be generated by the line stage in this 59/66cm chassis, it is necessary to provide a high HT voltage of 150VDC. This is fed into the line output transformer, T601, at pin 2 as shown in the diagram below, note that there is no feed resistor into the transformer.

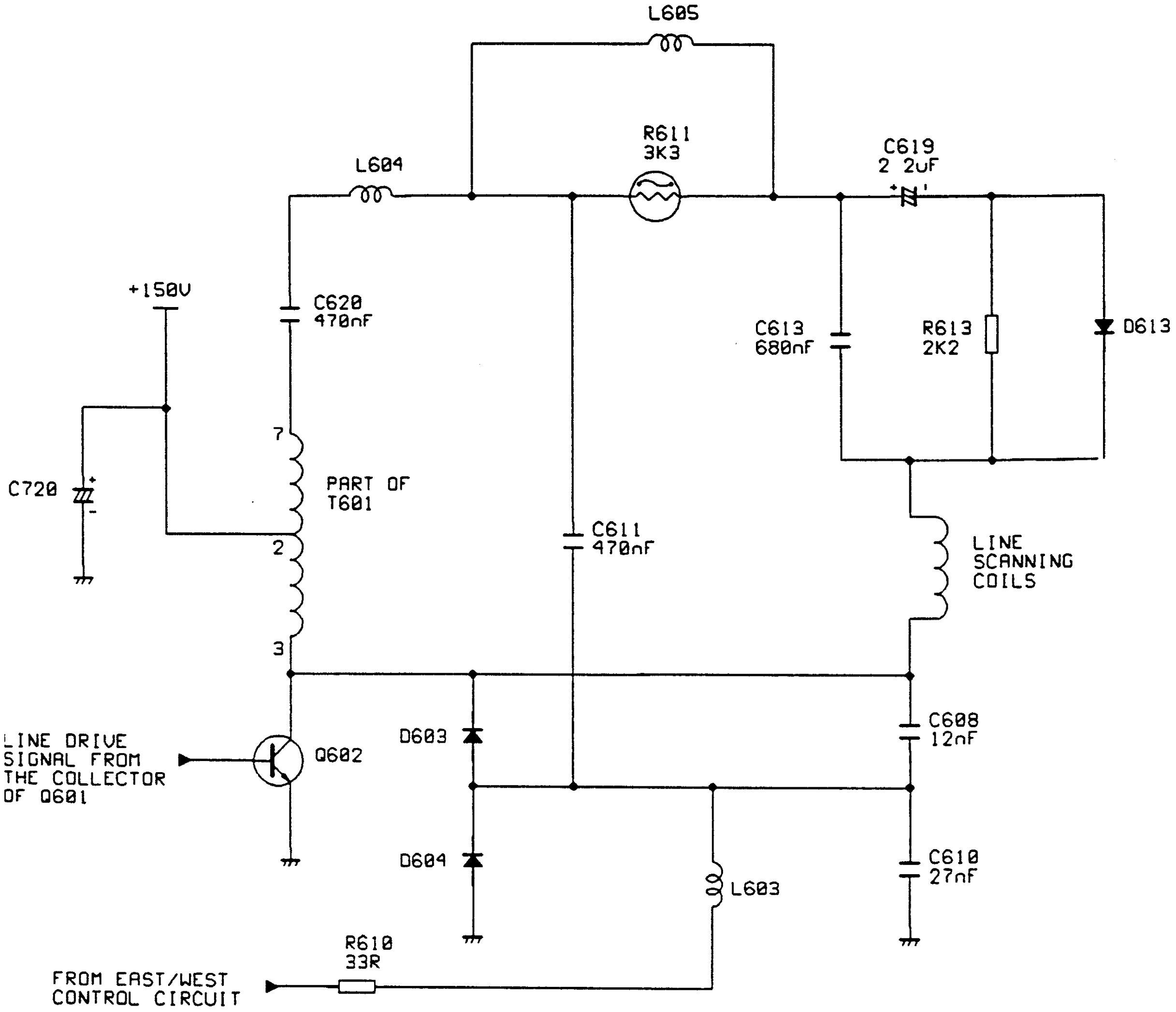
L605
R611
3K3
L604
C619
2 2uF
+150V
C620
470nF
C613
680nF
R613
2K2
D613
7
PART OF
T601
C720
C611
470nF
2
LINE
SCANNING
COILS
3
C608
12nF
LINE DRIVE
SIGNAL FROM
THE COLLECTOR
OF Q601
Q602
D603
D604
C610
27nF
L603
R610
33R
FROM EAST/WEST
CONTROL CIRCUIT

Figure 17 : Line Output Circuit

From the collector of the drive transistor, Q601, the line drive signal is fed into the base of Q602. This is a square wave signal that turns on for 26uS and off for 38uS.

When Q602 is turned on, current will start to flow in the primary winding of T601 (pins 2 to 3), this is point t1 in the current waveform shown on the next page. This current flow will continue to increase until Q602 is turned off some 26uS later, at which point the current in the primary winding will start to decay, point t2. The time taken for this current to decay is determined by the time constant of the primary winding and C608 (for the purpose of this explanation the bottom end of C608 and D603 can be considered to be ground and C610/D604 ignored). This charging current is supplied from the HT reservoir capacitor, C720, which will effectively connect pin 2 of the transformer to ground (for ac purposes).

At the point where the current starts to drive negative, t3, the clamp diode, D603 will start to conduct and thus stops the current going negative. The result of this is that C608 becomes a DC voltage source, which will discharge via the primary winding and C720, i.e. the current will start to increase again until it reaches point t4. This is were there is no energy left in C608 and the primary winding. At this point, 38uS after Q602 has turned off, Q602 will be turned on again and the cycle repeats.

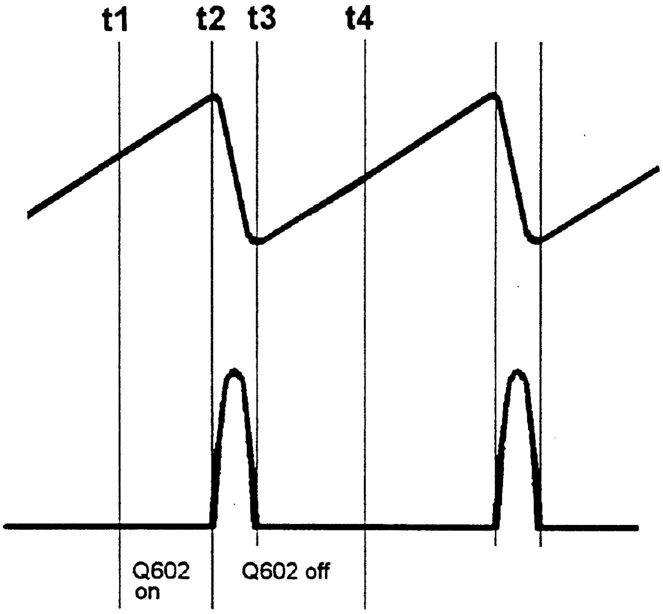

Figure 18 : Line Current and Voltage Waveforms (Idealised)

Note that as the voltage across the primary winding is proportional to the rate of change of current in it and since the rate of change is constant during the forward scanning stroke, but fast during the flyback period, the voltage across it (and the scanning coils) will be a series of pulse. This is also shown in the diagram below.

Also note that the above is an ideal explanation of the circuit operation, the actual waveforms generated will be somewhat different to those shown on the previous page.

Line scan correction

L605 provides for line linearity correction and R611 will damp any excessive voltage spikes across it, these spikes may cause striations on the left hand side of the screen if left undamped.

As the tube face is virtually flat, if the scanning current was not modified, this would result in the picture being cramped in the centre and stretched at the sides. To alleviate this it is necessary to compensate for the rate of change of the line scan current, i.e. to slow down the current at the start and end of scan. This can be achieved by fitting the correct value of capacitor in series with the line scanning coils. Normally referred to the S-correction capacitor, this is C613.

East/west correction is provided by the diode modulator and is explained in more detail in the **East/west correction** section of these notes.

Sand castle pulse

For correct internal processing within IC201, a reference pulse needs to be generated from the line and frame signals. This is referred to as the sand castle pulse and its wave shape is shown in the diagrams below.

To generate this pulse it is necessary to sample both the line and frame signals. The line pulse comes from the line output transformer, T601, and the frame pulse from the teletext processing IC, IC106. The line pulse generated from the line output transformer is rectified by D612, ensuring that only positive going pulses are present on its cathode. Connected to the cathode of D612 is D608 which is used to reduce the pulse by fifteen volts. This will ensure that the overall level of the line pulse will not exceed 5.5V when it arrives at pin 41 of IC201.

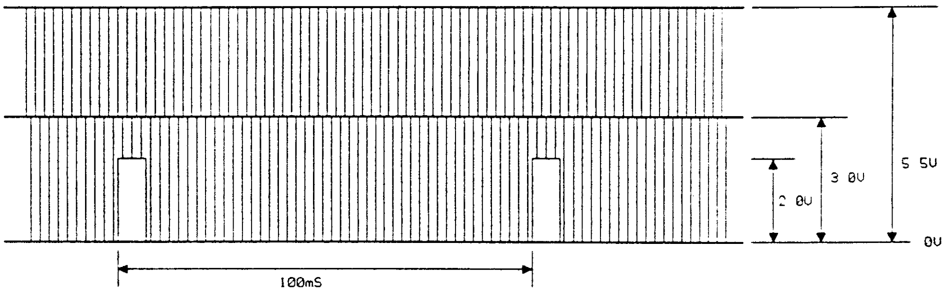

Figure 19 : Sand Castle Pulse

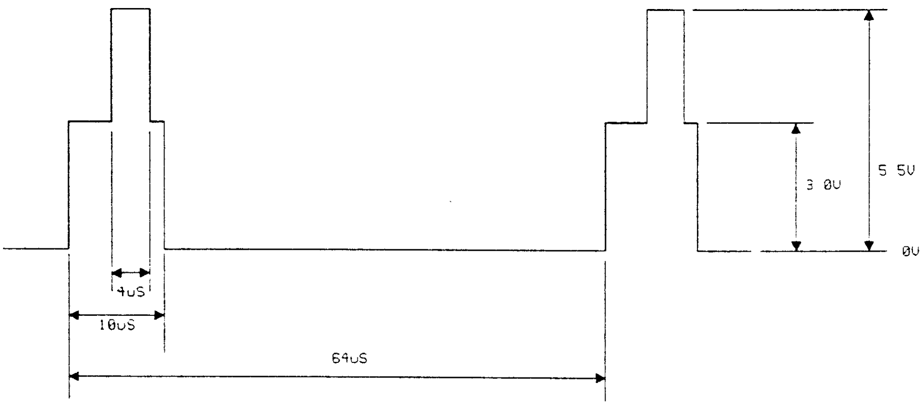

Figure 20 : Sand Castle Pulse Detail

R625 and R626 provide a load for the line pulse and R615 limits the current/voltage supplied. C618 suppresses any high frequency signals that may occur on the line pulse. These would be undesirable as they may cause unpredictable false triggering within IC201. D607 and D824 ensure that no erratic negative going pulses are present on the line signal. D813 ensures that the line pulse is pulled up to the +5V supply when present and to zero when not.

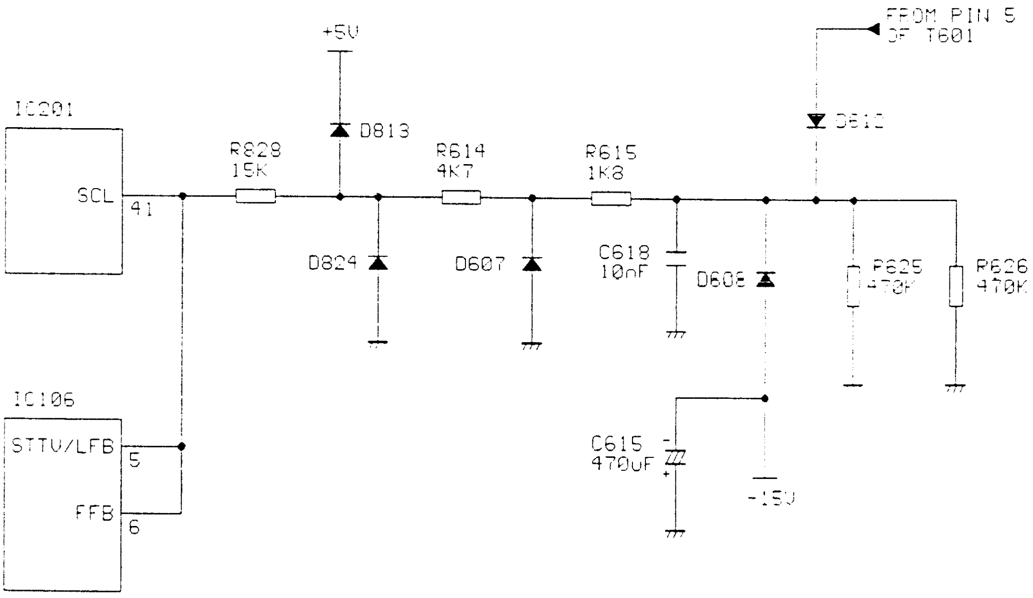
+5V
FROM PIN 5 OF T601
IC201
SCL
41
D813
R828 15K
R614 4K7
R615 1K8
D612
D824
D607
C618 10nF
D608
R625 470K
R626 470K
IC106
STTU/LFB
5
FFB
6
C615 470uF
-15V

Figure 21 : Sand Castle Pulse Generation Circuit

East/West correction

Principle of circuit operation

If the width of the picture were not varied during the line scanning process, it would result in a picture that would be wide at the top and bottom, but narrow as it progresses towards the centre. This effect is especially noticeable on large CRT's due to the distance the beam has to travel. The circuit used to correct for this distortion is called the east/west correction circuit and is described below.

At the end of line flyback time, the charge on C608 and C610 decays slowly to provide the first half of the scan. When the centre of the scan is reached Q602 will switch on and the scanning coils are supplied with current via the charging action of C613 (the S correction capacitor). Therefore, it can be seen that by changing the charge on C610, the width of the picture can be changed.

Circuit operation

Pin 45 of IC201 provides a parabola waveform at field rate that contains all the correction signals supplied from the NVM for picture geometry. This is added to the negative feedback signal from the output stage and is fed into IC502

IC502 (pins 1, 2 and 3) comprises a pulse width modulator whose non-inverting input, pin 3, determines the width of the pulse. The signal present on the inverting input of the amplifier is a ramp waveform, generated from a line pulse off the line output transformer.

At any instant in time, the voltage on the inverting input of IC502 will directly affect the timing of the signal on the output, i.e. when the ramp waveform crosses the threshold set by the parabola, the output of the amplifier will switch to a high level (see the diagram below). The maximum amplitude of the signal connected to pin 2 (ramp) is three volts and the maximum level of the signal on pin 3 (parabola) is one and a half volts. Therefore when the parabola is at its maximum level, the duty cycle of the output will be 50/50 and when the control voltage is lower the mark will increase to point set by its base line voltage.

Pulse width modulator

This ramp waveform is generated by the action of C516 and R519/520 under control of Q505. Initially the base of Q505 will be low and therefore C516 will be allowed to charge via R519 and R520. When Q505 is turned on as its base rises above 0.65V, the charging will stop and the capacitor will discharge via R520 and the collector/emitter junction of the transistor. Because the charge time is approximately eleven times that of the discharge time (R519 + R520 as opposed to just R520), the ramp will be gentle compared with the discharge.

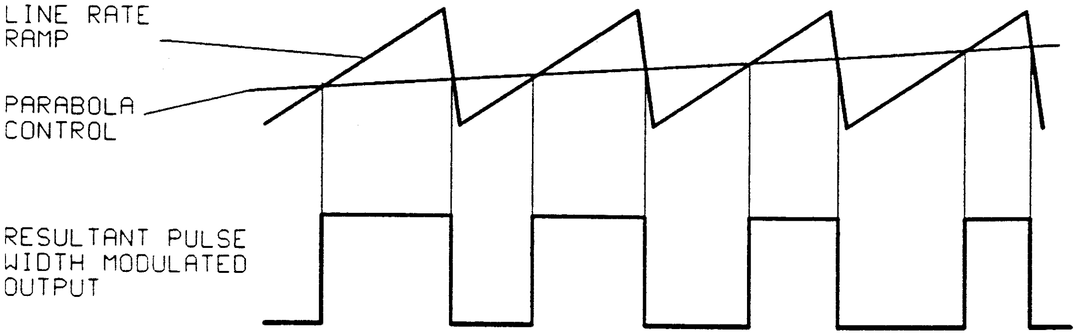

Figure 22 : IC502 Ideal Waveforms

Drive Circuit

This resultant pulse width modulated waveform is now fed into the base of Q506. The collector of this transistor is taken to the 150V supply via R526 and R527 which allows the voltage at this point to rise to approximately sixty volts. The actual signal generated is a pulse, whose width is dependant upon the on time of the pulse width modulated waveform, but as signal inversion takes place, the on time of the modulating signal will result in the off time of the pulse.

C610 provides the earth return for the line scanning coils, there will also be a pulse waveform at this the top of this capacitor will be in excess of 160V peak. The start point of the two waveforms on the cathode of D507 (60V peak) and the anode (160V peak) will occur at the same time, but the cathode will turn off sooner (determined by the modulating input signal of Q506). This being the case, the signal on the anode of D507 will be modulated with amplitude variations on each line pulse, and these variations will vary depending upon the point at which they occur in the parabola. The resultant waveform on the top of C610 will be a line pulse signal, modulated with the controlling parabola. This now meets our above criteria of changing the charge on C610 to vary the width of the picture during the frame scan.

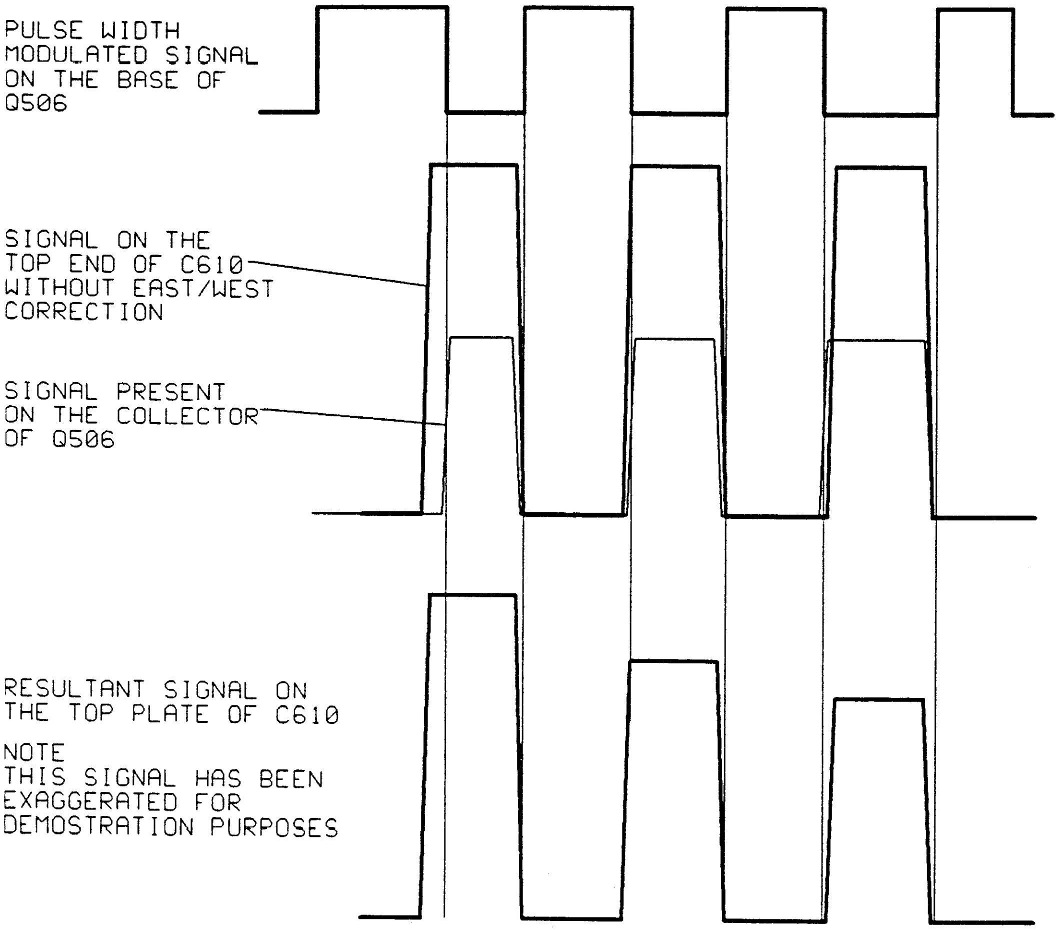
PULSE WIDTH MODULATED SIGNAL ON THE BASE OF Q506
SIGNAL ON THE TOP END OF C610 WITHOUT EAST/WEST CORRECTION
SIGNAL PRESENT ON THE COLLECTOR OF Q506
RESULTANT SIGNAL ON THE TOP PLATE OF C610
NOTE THIS SIGNAL HAS BEEN EXAGGERATED FOR DEMOSTRATION PURPOSES

Figure 23 : Idealised East/west Pulse Waveforms

As the east/west output circuit only requires power during the pulse part of its operation, it is possible to reduce the power dissipated by the circuit by using the circuit based around Q507. At initial start up, no voltage will be present in the east/west output circuit (because the line has not started up), so the +18V supply from the chopper stage is used to charge up C520. When the collector of Q506 goes high, it will turn on Q507 so that voltage can be supplied from C520. As the line stage starts up, the charge on C520 needs to be replenished quickly and this is done from the line output transformer itself (pin 6) via D516 and D519. D517 and D518 along with the +18V supply ensure that the voltage on the collector of Q507 does not exceed fifty four volts at any time.

D509 protects the collector emitter junction of Q507 should the pulses on the top of C610 become excessive.

A feed back circuit comprising of D508, R529, C517 and R523 provides negative feed back from the output of the driver stage. This is to prevent the circuit from oscillating, drawing too much current and causing damage to Q506 and Q507.

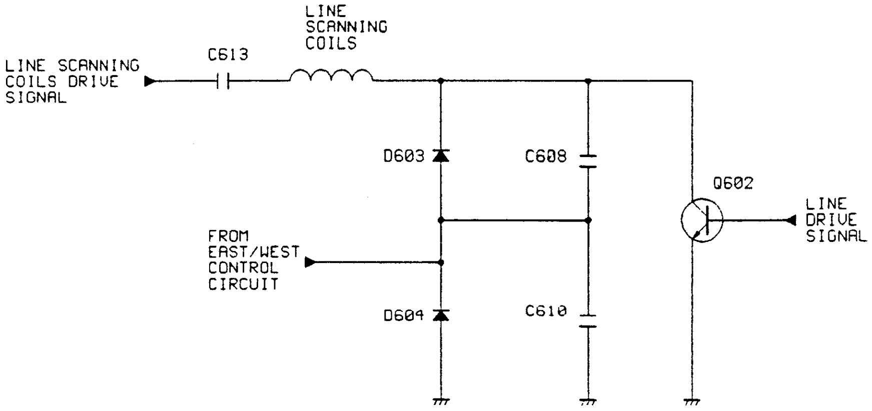
LINE SCANNING COILS
C613
LINE SCANNING COILS DRIVE SIGNAL
D603
C608
Q602
LINE DRIVE SIGNAL
FROM EAST/WEST CONTROL CIRCUIT
D604
C610

Figure 24 : Diode Modulator Circuit

The obvious advantage of this circuit configuration is that Q506 and Q507 are only conducting during the active line scanning period. This coupled with the fact that they are used as switches, i.e. maximum current/no voltage or no current/maximum voltage means that there is very little energy generated within these devices. Thus power consumption is kept down to a minimum.

Note that the east/west adjustment is made in the service mode and is referred to in the **Service set up mode** section of these notes.

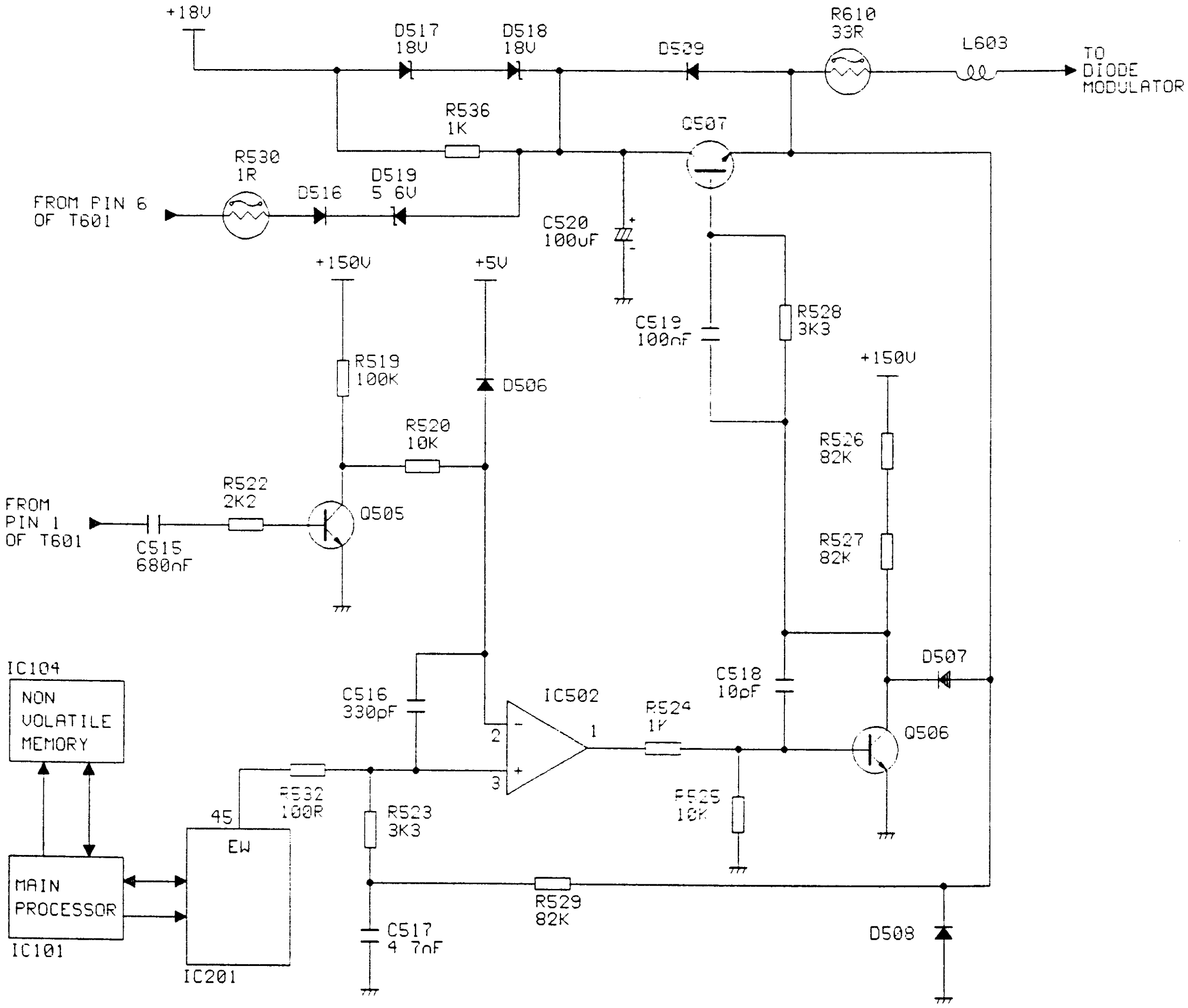
+18V
D517 18V
D518 18V
D509
R610 33R
L603
TO DIODE MODULATOR
R536 1K
Q507
R530 1R
D516
D519 5 6V
FROM PIN 6 OF T601
C520 100uF
+150V
+5V
C519 100nF
R528 3K3
R519 100K
D506
+150V
R520 10K
R526 82K
R522 2K2
FROM PIN 1 OF T601
Q505
C515 680nF
R527 82K
IC104
NON VOLATILE MEMORY
D507
C518 10pF
C516 330pF
IC502
R524 1K
Q506
2
1
3
R532 100R
R525 10K
45
EW
R523 3K3
MAIN PROCESSOR
IC101
R529 82K
C517 4 7nF
D508
IC201

Figure 25 : East/West Drive Circuit

Supplies generated by the line stage

A number of conventional supplies are generated from the line output transformer, EHT, Focus, G2, A1 and CRT heaters. A further +/- 15V is also generated for the vertical output stage. Also there is a +2V supply for the east/west diode modulator and a -10V supply which along with the +2V supply is used to drive the line output transistor. See the **Line drive circuit description** section of these notes for more details on this.

Supply Name	Voltage (approx)	Purpose	Point of Generation
EHT	28kV	CRT final anode	Top of split diode chain
Focus	8kV	CRT focus grid	Split diode chain
G2	500V	CRT grid	Split diode chain
CRT Heaters	3VAC	CRT Heaters	Pin 1 of T601
+45V	+45V	East/west correction circuit supply	D510, Pin 6 of T601
+45V	+2.0V	Line drive	D605, Pin 10 of T601
+15V	+15V	Vertical output supply	D609, Pin 9 of T601
-15V	-15V	Vertical output supply	D608, Pin 5 of T601
-45V	-10V	Line drive	D602, Pin 6 of T601

As the +/-15V supplies are generated by the line stage, there will be no vertical scanning or sound output until these have come up (note that the sound output stage is supplied from the chopper +/-18V supplies, but no current will be supplied until it starts to amplify the output from IC305, this is muted until the line stage is fully functional). Also the +45V supply will not be established until the line stage is running. This effectively ensures that the line stage 'soft starts' and therefore significantly reduces the risk of component failure as the receiver is turned on, i.e. current is taken from the chopper supply in the following time sequence :-

1. Line stage starts up at 31.25kHz using the -18V and +13V supplies from the chopper.
2. Feed back is received from the line stage and IC201 switches to 15.625kHz.
3. Line stage runs (+150V from the chopper and -10V/2.0V from line stage).
4. Vertical stage starts up using the +/-15V supplies from the line stage.
5. Current is drawn for the sound output stages as the output from IC305 is turned on.
6. RGB drive is turned on and current is drawn from the +150V supply from the chopper by the CRT drive IC.

Note that the CRT drive amplifier is not supplied from the line output stage, as in other Sharp television chassis, but is derived direct from the 150V supply generated by the chopper stage.

Beam current limiter

Beam current limiting is carried out to remove the risk of forward X-ray emissions, to stabilise the EHT and control picture brightness. Feedback to control the beam current is taken from the bottom end of the EHT over winding as shown in the diagram below.

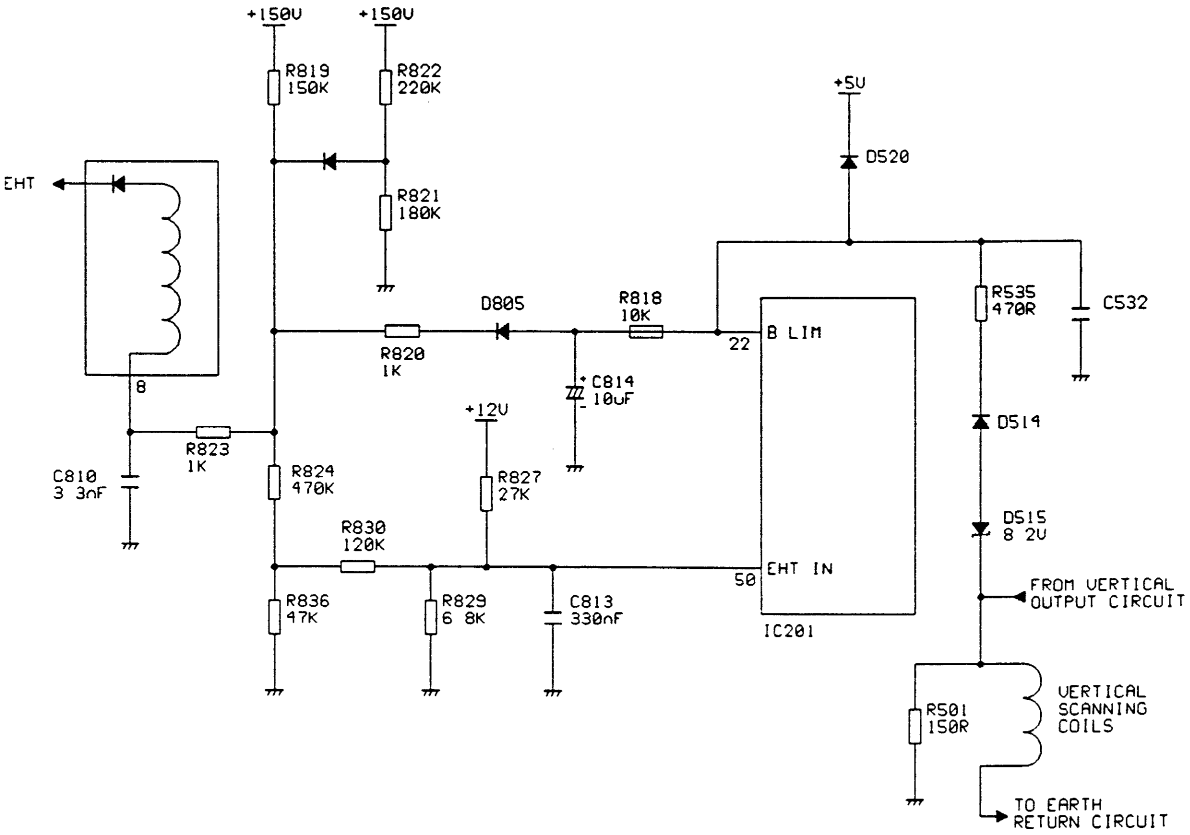
+150V
+150V
R819
150K
R822
220K
+5V
D520
EHT
R821
180K
D805
R818
10K
R820
1K
22
B LIM
R535
470R
C532
8
C814
10uF
+12V
D514
C810
3 3nF
R823
1K
R824
470K
R827
27K
R830
120K
D515
8 2V
EHT IN
50
R836
47K
R829
6 8K
C813
330nF
IC201
FROM VERTICAL OUTPUT CIRCUIT
R501
150R
VERTICAL SCANNING COILS
TO EARTH RETURN CIRCUIT

Figure 26 : Beam Current Limiter Circuit

Feed back for the beam current limiter is taken from the bottom end of the EHT over winding on pin 8 of T601. This produces a DC voltage which is fed into pins 22 (B LIM) and 50 (EHT IN) of IC201. When the beam current increases, the voltage on pin 8 of T601 will rise, conversely as the beam current decreases the voltage on this pin drops.

Beam limiting input of IC201

Pin 22 (B LIM) will ensure that the picture brightness is maintained within limits should the beam current increase or decrease by varying the amplitude of the video signal. Should the beam current become excessive, then IC201 will reduce the amplitude of the video signal so that the screen blanks out (raster still present, but no picture). If the beam current then increases still further, the video signal will be reduced below the black level to give an ultra black picture.

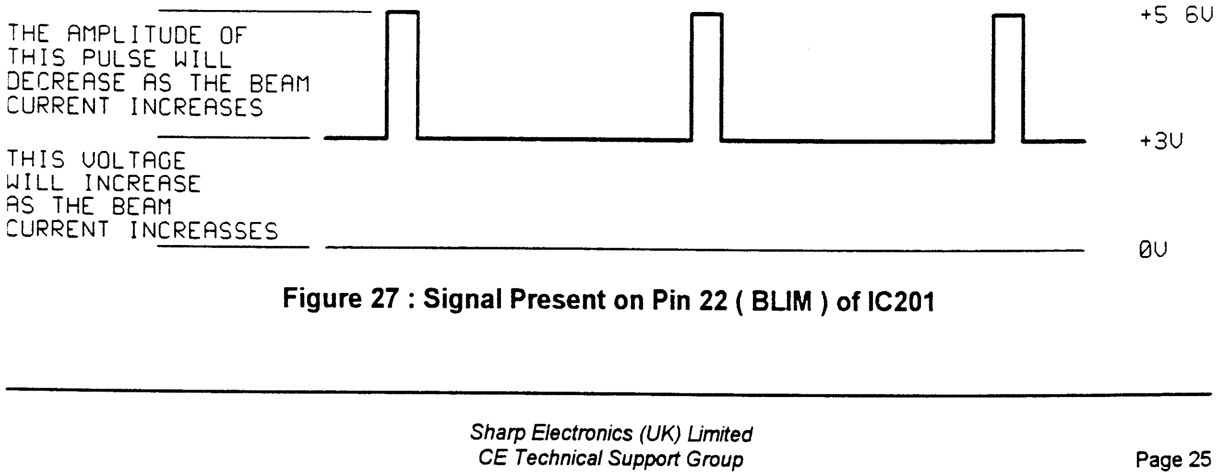

Figure 27 : Signal Present on Pin 22 (BLIM) of IC201

The signal on pin 22 is a pulse (at vertical rate) sitting on a DC pedestal of three volts (nominal value as this varies anywhere between +1V and +4V).

Vertical circuit failure - CRT protection

If the vertical drive were to stop, a bright white vertical line will appear across the centre of the CRT. This is obviously undesirable as it may burn the phosphor coating if left on for too long. To alleviate this possibility a feed is taken from the vertical output (top end of the vertical scanning coils) via D515. D515 ensures that only signals greater than 8.2V pass to pin 22. D514 provides isolation and D520 clamps pulse to a maximum level of five volts.

Under normal conditions this has no effect on the operation of the beam current limiter. When the vertical drive signal falls below 8.2V (flyback pulse) the pulses developed at the cathode of D514 will disappear and this will cause the screen to go ultra black, ensuring that no damage is done to the CRT. In this situation, if the beam current is increased by turning up the G2 control on T601, a thin horizontal white line will be seen momentarily unit the beam current limiter circuit compensates and turns the current down again.

EHT input of IC201

If the beam current increases significantly, then there will be a risk of forward X rays being generated from the CRT face. To prevent this condition, pin 50 (EHT IN) is used to monitor for excessive beam current.

Although the B LIM pin will reduce the risk of forward emissions, as it only changes the video signal, the EHT IN pin will override this operation. When active, i.e. X ray emission may be possible, pin 50 will return the set to standby. This pin is nominally 2VDC, but this will change slightly with beam current.

Vertical Stage

Vertical time base generation

A R/C oscillator within IC201 provides a vertical drive signal for the vertical drive and output stages . External components are used to control the stability and phasing of this signal (note that the external crystal is not used as a reference source - the vertical stage will operate with this component disconnected from the circuit) When a video signal is present, this oscillator is locked to the incoming vertical synchronisation pulse.

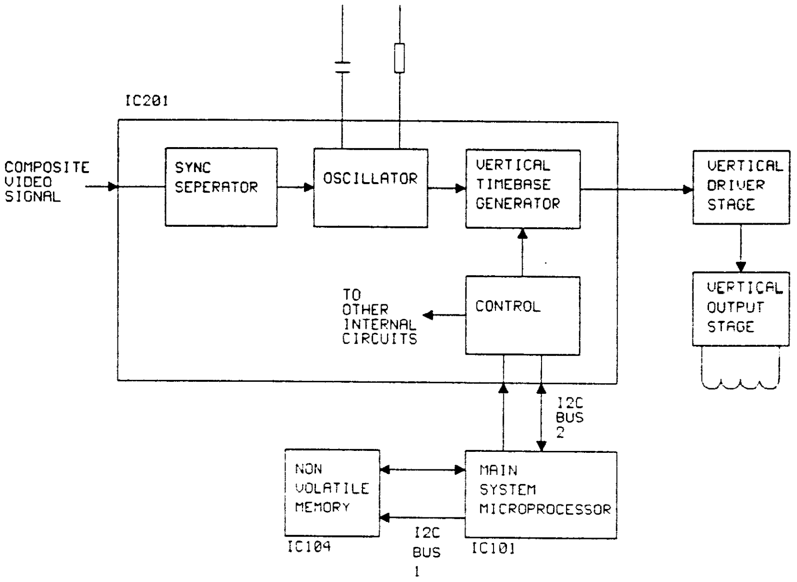

Figure 28 : Vertical Stage Block Diagram

The oscillator has two outputs that exit IC201 from pins 46 (V OUT P) and 47 (V OUT N). Pin 47 provides the main drive signal, while pin 46 provides the correction signal, i.e. the vertical geometry signal. The geometry settings are contained within the non volatile memory and are accessed via the I^{2}C bus and the microprocessor.

As can be seen from the diagram on the next page, the vertical drive signals from IC201 pass into the operation amplifier IC502 on pins 5 and 6. This amplifier sums the two inputs, the resultant output being fed into pin 6 of IC501. Feed back from the vertical stage comes from the bottom end of the vertical scanning coils via R516 and R539. This is to ensure that the vertical stage does not drive the coils incorrectly due to inefficiencies within the vertical drive or output circuits, i.e. it provides negative feed back. Also connected to this feed back point is the output from pin 47 of IC201, this pin is effectively the frame correction signal.

The input to the second operational amplifier, IC501, is also affected by the vertical scanning coils drive signal (top end of the vertical scanning coils). This enters via R511 (to the inverting input on pin 6) and R509 (to the non-inverting input on pin 5). This provides positive feed back and therefore will cause the stage to oscillate. This oscillation is free running, but remains at about 140kHz (this is set mainly by C509 and R509). The output from pin 7 is a square wave whose frequency and mark/space ratio is dependant upon a number of factors. One is the drive signal itself, two the frame geometry settings and three the frequency of oscillation generated by the feedback to IC501. This signal then drives Q503 and Q504 in the frame drive circuit described in the next section.

Both IC501 and IC502 are supplied on pin 8, +5V and 4, -15V. This ensures that the output from pin 7 of IC501 is swinging both positive and negative.

Vertical geometry is set using the software service mode and therefore all adjustments are stored in the NVM, IC104. Please refer to the **Service Set Up Mode** section of these notes for information on how to set the geometry of the vertical stage output.

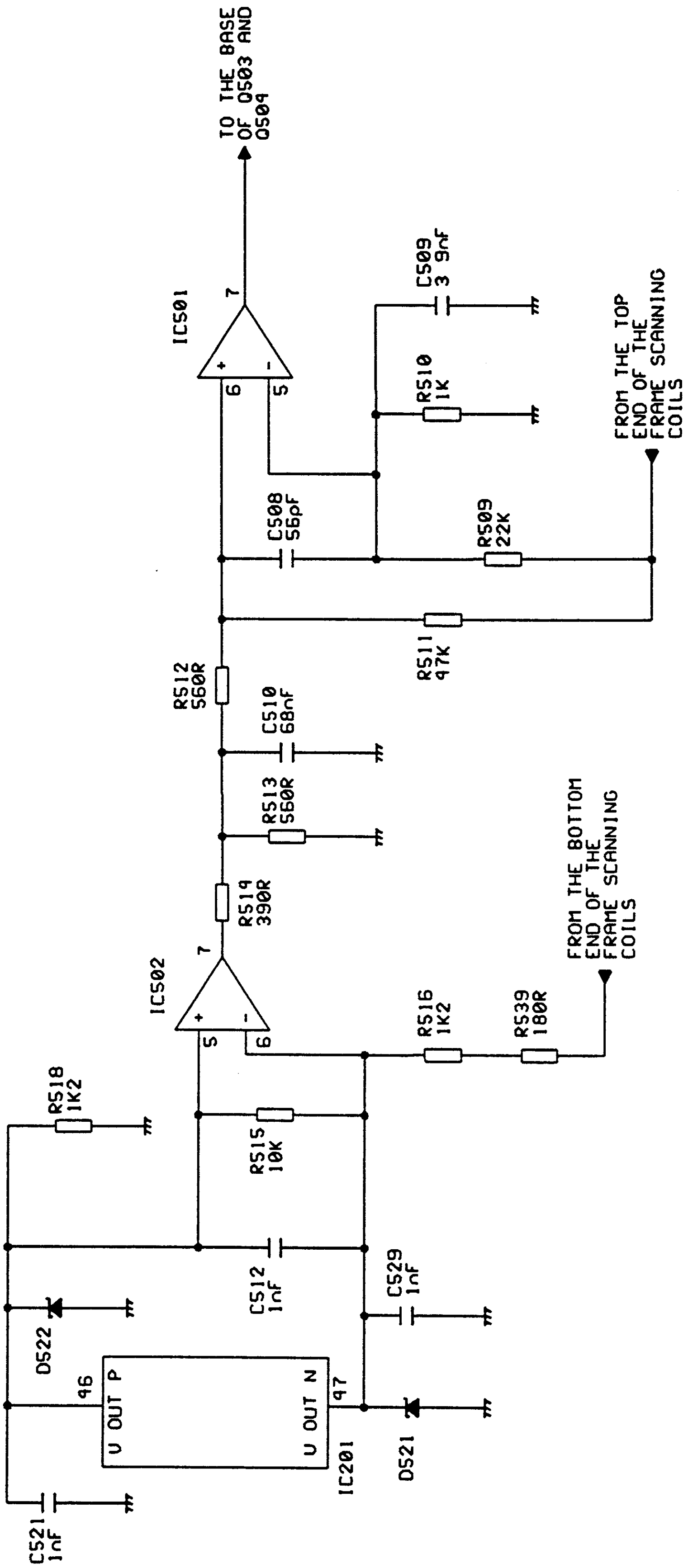
TO THE BASE OF Q503 AND Q504
IC501
7
6
5
+
-
C509 3.9nF
R510 1K
FROM THE TOP END OF THE FRAME SCANNING COILS
C508 56pF
R509 22K
R511 47K
R512 560R
C510 68nF
R513 560R
R519 390R
IC502
7
5
6
+
-
FROM THE BOTTOM END OF THE FRAME SCANNING COILS
R516 1K2
R539 180R
R518 1K2
R515 10K
C512 1nF
C529 1nF
D522
46
V OUT P
V OUT N
47
IC201
D521
C521 1nF

Figure 29 : Vertical Drive Circuit

Vertical scan coil drive circuit

The vertical output stage used in the CA10 chassis is based around two field effect transistors - Q501 and Q502. As power consumption and therefore heat generation needs to be kept to a minimum a class D amplifier type configuration is utilised. This basically means that the FET's are used as switches to switch either the +15V or -15V into the output load (in this case a low pass filter) then into the vertical scanning coils. This is based upon the fact that the input signal from the drive amplifier is a pulse width modulated signal whose base frequency is 140kHz.

Transistors Q503 and Q504 ensure that the drive signal present at the junction of Q503 emitter and the collector of Q501 (marked as point A in the circuit diagram on the next page), swings between -14.4V and +4.4V. When the drive signal is high (positive), Q503 will be turned on and point A will be +4.4V. When the drive signal is low (negative) then Q504 will turn on and point A will be -14.4V. This is necessary to ensure that the output FET's are operating in their fully saturated states, if they were not fully saturated then the circuit would become inefficient and heat would be generated eventually resulting in the failure of the FET's.

Note that D511 ensures that the voltage on the collector ofQ505 does not exceed 6.8V as any voltage greater than this will damage the device. Q503 and Q504 are emitter followers and as such their emitters will follow the base voltage, therefore if there is too large a volt drop across the collector/emitter junctions of these transistors they will fail.

When point A is at +4.4V, the zener diode D504 will be forward biased and therefore current will flow from the -15V supply via D513 and R505. The gate of Q502 will rise to -6.8V and turn it on and effectively connect the -15V supply to the output load. At this time the other FET, Q501 will be turned off as its gate will be +15V by the pull up action of R504 and D512 (D503 is not conducting).

When point A changes to -14.4V, Q502 will turn off as D504 ceases to conduct and its gate voltage will drop to -14.4V by the action of the pull down of R505 and D513. At the same time, D503 will become forward biased resulting in a voltage of +7.6V on the gate of Q501 which is enough to turn it on and connecting the +15V supply into the load.

It is vitally important that both Q501 and Q502 are not turned on at the same time as excessive current will flow between the positive and negative fifteen volt lines resulting in the FET's going short circuit and the supply feeds going open circuit. To ensure that this does not occur, each FET needs to be held off momentarily until the other one has stopped conducting. This is achieved by the capacitors connected across D503 and D504.

When Q501 is conducting, the voltage on the gate of Q502 will be held at -15V, keeping it turned off. As the polarity of point A changes and Q501 is turned off, C523 will retain enough charge to hold the gate of Q502 at -14.4V until Q501 is turned fully off. The reverse occurs when Q502 turns off, but this time capacitor C506 is used to keep Q501 off. This happens as it takes a small amount of time to charge each capacitor during the cycle, therefore if the value of the capacitor goes down, or one goes open circuit, the FET's would over heat or in worst case expire. By holding off the conduction of Q501 and Q502 momentarily cross over distortion will occur. In a conventional amplifier this is undesirable as it will cause distortion in the output signal. However, as the output signal passed through a low pass filter to recover the original frame scanning signal, this cross over distortion can be ignored, i.e. it has no effect on the drive signal.

From the source of Q502/drain of Q501 the amplified pulse width modulated drive signal passes into a low pass filter comprising of L504, L505, C502, L502 and C504. This has the effect of removing the oscillation of 140kHz and leaves the vertical drive signal at 50Hz. This voltage is now fed into the vertical scanning coils via the socket assembly.

Note that as the positive and negative fifteen volt supplies are generated by the line stage, there will be no frame scan until the line stage has come up.

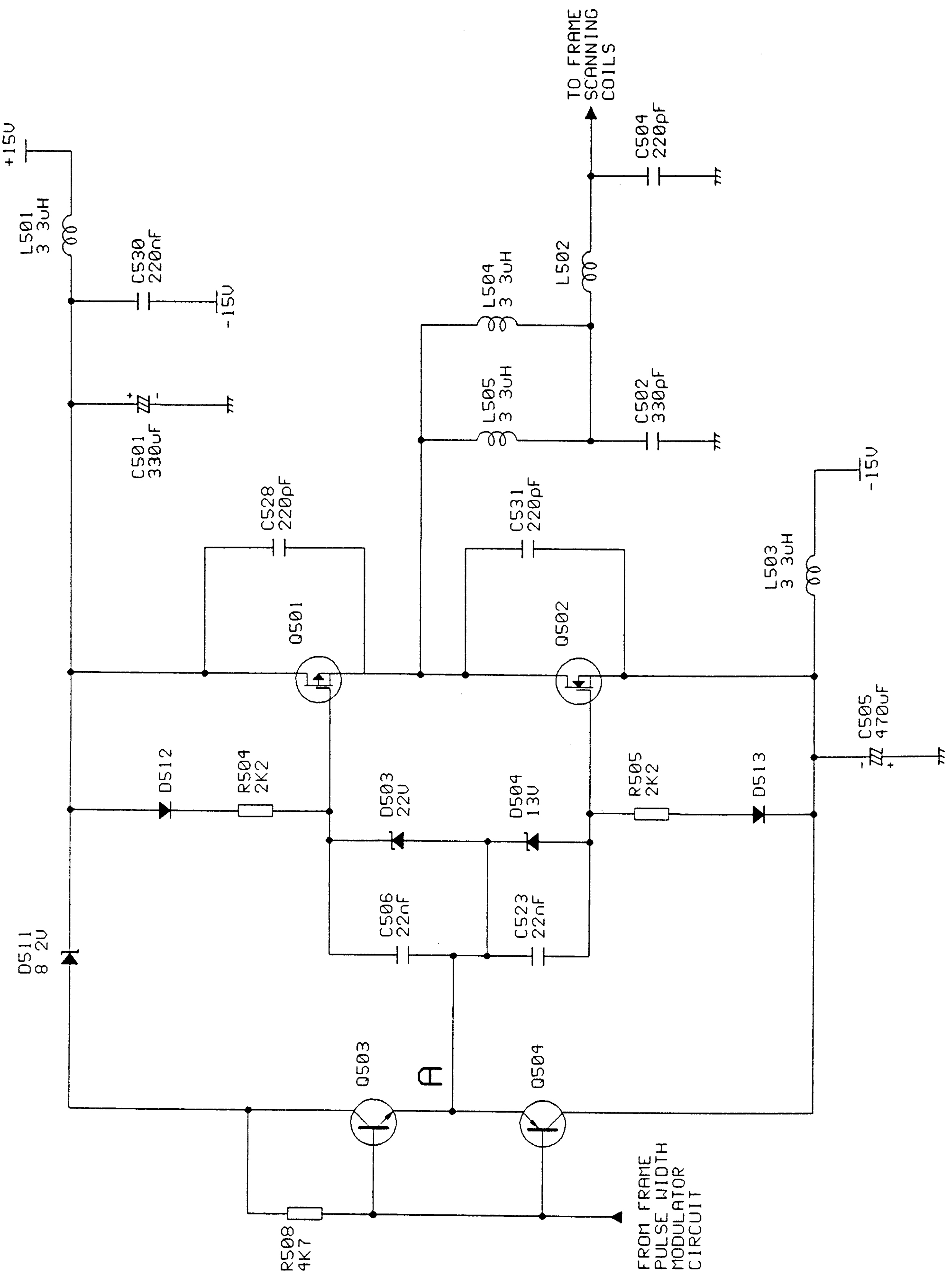
+15V
L501
3.3uH
C530
220nF
-15V
C501
330uF
C528
220pF
Q501
D512
R504
2K2
D511
8.2V
D503
22V
C506
22nF
Q503
A
R508
4K7
L504
3.3uH
L505
3.3uH
L502
C504
220pF
TO FRAME
SCANNING
COILS
C502
330pF
C531
220pF
Q502
D504
13V
C523
22nF
Q504
FROM FRAME
PULSE WIDTH
MODULATOR
CIRCUIT
-15V
L503
3.3uH
C505
470uF
R505
2K2
D513

Figure 30 : Vertical Output Stage

Tuner and IF

Tuning and IF control is provided by the system microprocessor, IC 101 via the I²C bus line. The tuner itself is a digitally controlled device, which eliminates the need for a separate VT line generator circuit. As the tuner is controlled directly from the microprocessor, it is easier to provide direct channel entry and as an added feature the set is also equipped with auto channel sorting. This is across the normal UK channel band and cable channels.

Most of the IF circuitry is contained within IC201 (Video IF) and IC305 (Audio IF), the minimal amount of external components provide for IF signal filtering - see **IF signals** section for more details.

Tuner and IF processing

All IF processing is carried out within either IC201 for video or IC305 for audio. Initially the IF from the tuner enters IC201 and is decoded to produce the base band signal - see the spectrum diagram shown later in these notes. As this is a composite of the video and audio IF (FM and NICAM) signals it is necessary to process it further to ensure that no corruption occurs in the later stages. The circuit shown below serves this function.

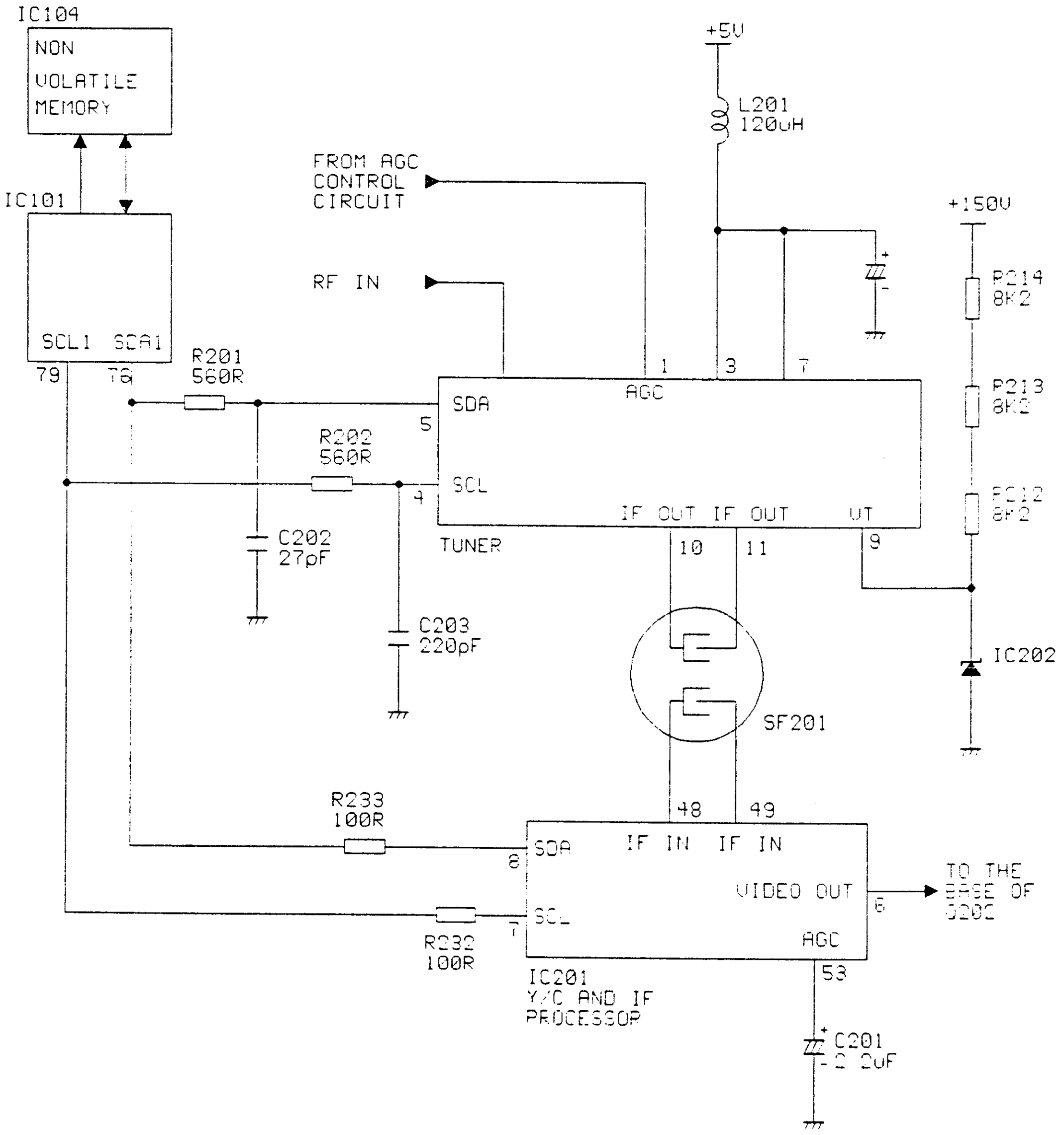
IC104
NON VOLATILE MEMORY
IC101
SCL1 SDA1
79
78
R201 560R
R202 560R
C202 27pF
C203 220pF
FROM AGC CONTROL CIRCUIT
RF IN
+5V
L201 120uH
+150V
R214 8K2
R213 8K2
R212 8K2
SDA
SCL
AGC
IF OUT IF OUT
UT
TUNER
1
3
7
5
4
10
11
9
SF201
IC202
R233 100R
R232 100R
48
49
SDA
SCL
IF IN IF IN
VIDEO OUT
AGC
8
7
6
53
TO THE BASE OF Q202
IC201 Y/C AND IF PROCESSOR
C201 2.2uF

Figure 31 : Tuner and IF Signal Path

When the user selects an off air signal, data is taken from the NVM and used by the microprocessor to generates the data signal fed into the tuner. This data will control the digital to analogue converter contained within the tuner module so that the correct voltage is applied to the varicap diodes. Like most tuners it is necessary to provide a 32 volt supply line to allow for total band coverage of the tuning voltage, this is provided from the +150 volt line via the dropper resistors R211, R213 and R214 and IC202. IC202 is effectively a 32 volt high stability zener diode.

Other supplies need to be present to make the tuner work correctly. Although there is only one other supply source (+5V) this is used internally for the digital to analogue converter, RF amplifier, tuning stages and IF processing circuits. The low pass filtering circuit on the supply line comprising of L201 and C204 ensure that no high frequency noise enters the tuner, this could lead to the tuner oscillating erratically resulting in picture corruption.

Once the tuner has tuned into a channel, the IF signal output passes out of pins 10 and 11 via the SAWF filter, SF201, and into the main IF amplifier contained within IC201. IC201 then further amplifies the signal and converts it into a composite baseband signal.

Automatic frequency control

To keep the station on tune at all times, an automatic frequency control system is utilised. Once again this circuit is based around the system microprocessor. Unlike previous chassis, there is no external AFC circuitry, as all the processing is done within IC101 and IC201. If it is seen the signal is going off tune, then the microprocessor will change the RF tuning point within the tuner via the I^2C bus line. The reference for the AFC circuit is maintained by the detector coil T201, which has to be correctly set to ensure that the set does not drift off tune on off air broadcasts.

Tuning features

As this receiver uses a digitally controlled tuner, it is possible to add some advanced user features to the receiver. Direct channel entry is possible using the remote control and auto sort tuning is provided.

As the receiver leaves the factory, the auto sort tuning feature is enabled, this is so that the end user does not have to manually tune the unit in when getting it home. When the receiver is first turned on, the end user is presented with a screen that instructs them to connect the aerial, VCR (while playing a tape) and satellite receiver (switched on and tuned to a station) to the rear of the set via the RF socket. They are then requested to press any button on the remote control, the auto tuning/sorting sequence will now be initiated.

First the signal carrier is detected, then the sync detector detects a line sync signal and the tuning operation slows down and the signal is fine tuned, both of these operations are contained within IC201 and control is maintained by IC101 via the I^2C bus 2. Next the teletext header is decoded by IC106 and the time taken to decode it is stored within the NVM, IC104, via the I^2C bus 1. The data value relating to the VT line voltage is also stored. This process continues for all channels.

When this process is completed the text header (if transmitted), time taken to obtain the text header and tuning point will all be stored in the NVM. The set will now sort this information depending on the text header and time taken to obtain the text header. Contained within the EPROM, IC105 is the instructions to store BBC1 on PR1, BBC2 on PR2, ITV on PR3, Channel 4 or SC4 on PR4 and Channel 5 (if being transmitted) on PR5. As the VCR was playing a tape (no text header) this will be put on CH6 and any other equipment connected at RF will be put on the next available program numbers.

As the receiver may pick up signals from other transmitters, it is necessary for the system processor to decide which ones are more desirable to put in the first positions. This is done by examining the time to decode up the text header. The faster the text header is decoded, the stronger the signal and so the strongest broadcast is stored in the primary position for that station. As it is possible that the incorrect station may be stored in the primary position, i.e. Carlton ITV instead of Meridian ITV, a tuning editing menu is provided so that the end user can change this.

Note that any stations that are too weak to be stored in the primary positions are stored in the remaining free locations after the VCR and satellite channels (if connected). For a circuit description of this process, please refer to the **Automatic tuning circuit operation** section of these notes.

IF signals

From pin 6 of IC201, the base band signal (a frequency spectrum of the base band signal is shown on the next page) passes into the emitter follower, Q202. This ensures that the signal is matched to the following stages and allows buffering from the output of IC201. From the emitter of Q202, the signal splits into two paths. The first path goes into the base of Q203 via the a 6MHz filter CF202 which removes the audio IF signals from the composite video signal, the second path is via C304 and the high pass filter C334, L302, C335 and R309 into the base of Q301 which removes the video signal from the audio IF signal.

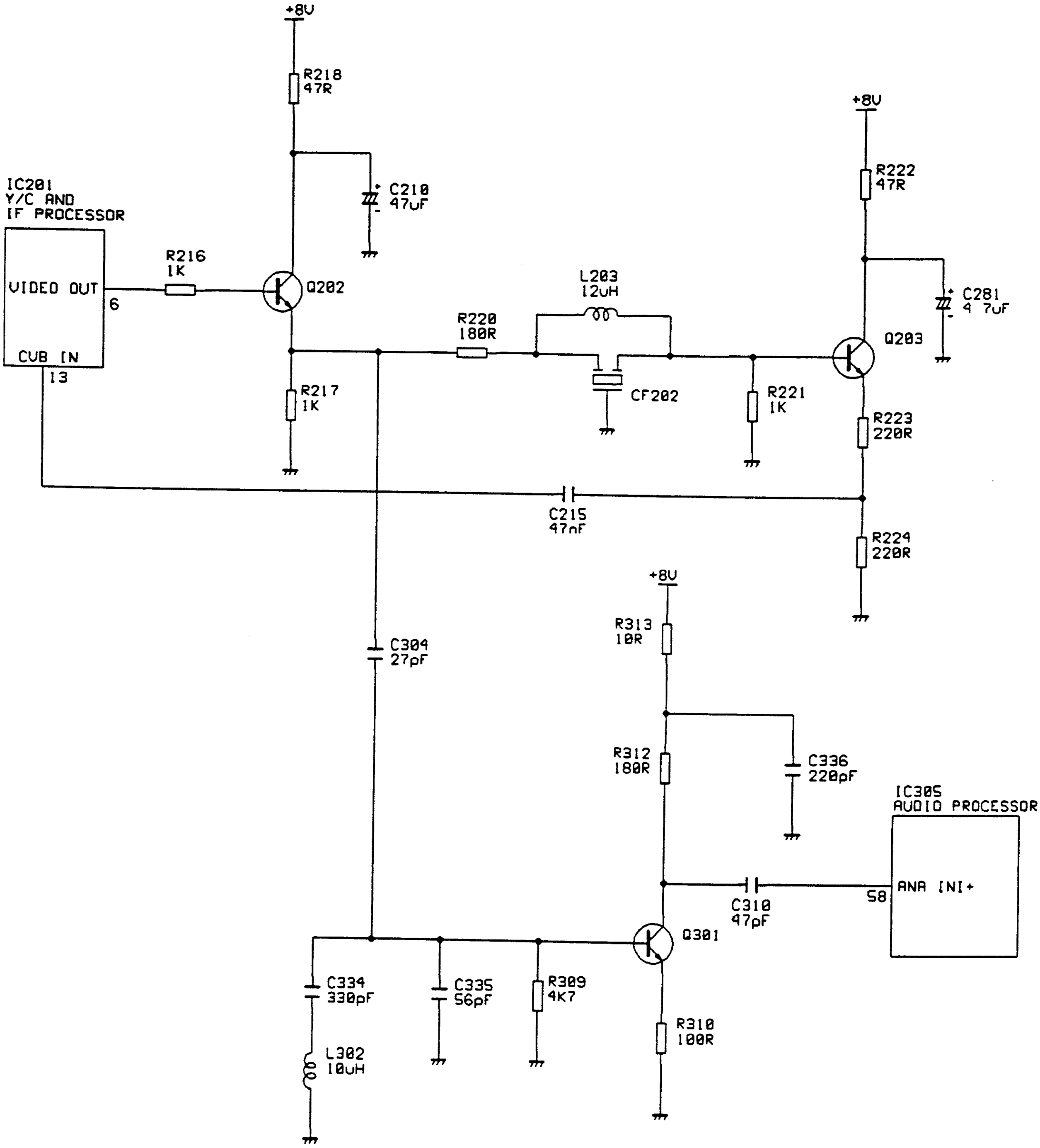
+8V
R218
47R
+8V
R222
47R
IC201
Y/C AND
IF PROCESSOR
C210
47uF
R216
1K
VIDEO OUT
6
Q202
L203
12uH
C281
4.7uF
R220
180R
Q203
CVB IN
13
CF202
R217
1K
R221
1K
R223
220R
C215
47nF
R224
220R
+8V
R313
10R
C304
27pF
R312
180R
C336
220pF
IC305
AUDIO PROCESSOR
ANA IN1+
58
C310
47pF
Q301
C334
330pF
C335
56pF
R309
4K7
R310
100R
L302
10uH

Figure 32 : Video/Audio IF Split

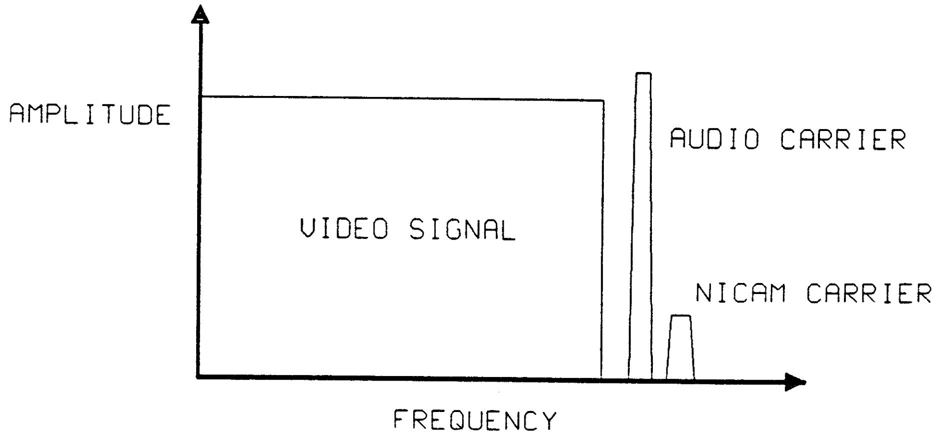

Figure 33 : Spectrum of the Base Band Signal

Each signal path from IC201, pin 6 will now explained in more detail below.

Audio IF processing

C304, being of a very small capacitance, will only pass relatively high frequencies which will effectively remove any signals below about 5MHz. This coupled with the filtering network of C334, L302, C355 and R309 (effectively a high pass filter) will ensure that only the audio FM carrier at 6MHz and the NICAM carrier at 6.522MHz pass into the base of Q301. Q301 amplifies the resultant audio IF and this signal is then coupled via C310 into the audio processor, IC305, at pin 58 (ANA INI+). C336 ensures that no IF signal passes onto the supply.

IC305 contains further IF amplification and the decoder stages to recover both the mono FM and stereo NICAM signals. Switching is carried out automatically within the IC. The receiver will automatically default to the stereo (NICAM) signal, but this can be over ridden by the end user by the use of a menu option. Note that when in the stereo mode, SRS and Dolby can be used, but in the mono mode only stereo wide is available.

For details on the audio switching circuits, please refer to the **Audio Processing** section of these notes.

Video IF and signal processing

All the video IF circuitry is contained within IC201, the output on pin 6 (VIDEO OUT) is a base band signal as shown in the above diagram.

From the emitter of Q202, the base band signal is passed through CF202 and L203. These components effectively comprise a 6MHz trap and will remove any signals in the audio IF range (FM and NICAM sound carriers), thus the signal entering the base of Q203 will be the video signal. R220/R217 and R221 ensure that correct impedance matching is provided to CF202.

Q202 is an emitter follower which gives the correct impedance match and drive signal back to the video processing circuits contained within IC201. C281 ensures that no video signal appears on the supply line.

From pin 13 (CVB IN) of IC201, the video signal is decoded and passes out of the IC as an RGB signal to drive the CRT via IC901.

RF AGC operation

As signals received from off air transmissions can vary tremendously from area to area, it is necessary to provide some form of automatic gain control on the incoming RF signal. The circuit shown below performs this action.

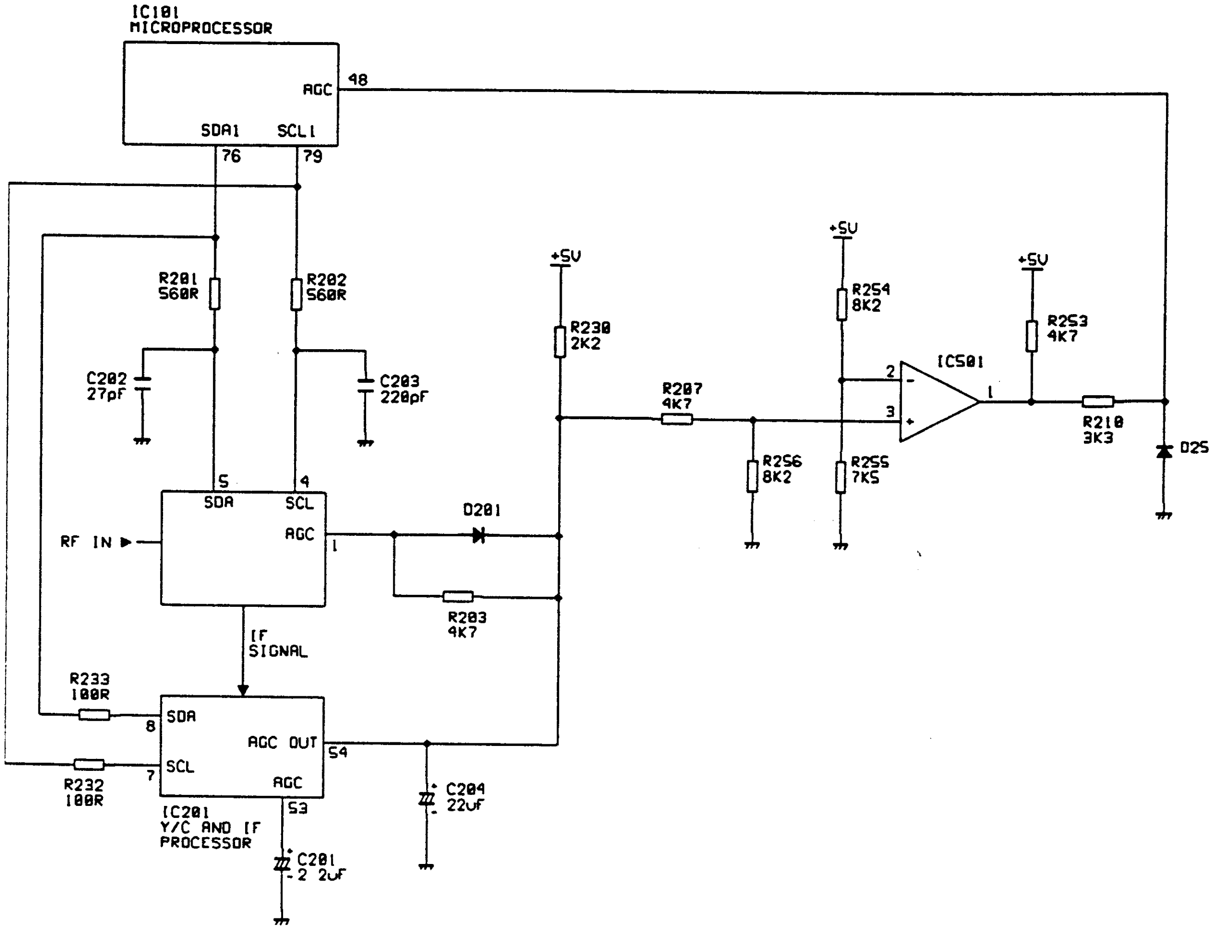
IC101
MICROPROCESSOR
AGC
48
SDA1
SCL1
76
79
R201
560R
R202
560R
C202
27pF
C203
220pF
5
4
SDA
SCL
AGC
1
RF IN
D201
R203
4K7
IF
SIGNAL
R233
100R
8
SDA
AGC OUT
54
7
SCL
AGC
53
R232
100R
IC201
Y/C AND IF
PROCESSOR
C201
2 2uF
C204
22uF
+5V
R230
2K2
R207
4K7
R256
8K2
+5V
R254
8K2
R255
7K5
IC501
2
3
1
+5V
R253
4K7
R210
3K3
D251

Figure 34 : Automatic Gain Control Circuit

It can be seen the at the heart of the system is the main system microprocessor, IC101. Via the clock and data lines, IC101 will instruct the tuner to tune to the desired signal (the data for this operation would have been set by the user at the initial installation and the control values held within the non volatile memory, IC104). The signal from the tuner will enter IC201 (video IF) in which there is a detection circuit which will give out a DC voltage on pin 54 (AGC OUT) that is dependant upon signal strength. This is fed straight back into the tuner AGC pin which will first control the gain of the RF stages within and then the IF stages, i.e. maximum gain is always given to the RF amplifier to reduce noise.

Automatic tuning operation

During the automatic tuning function it is necessary to detect the presence of a signal. While this is done by detecting the presence of a valid carrier signal, it is also necessary to monitor the amplitude of the RF signal to ensure that the RF signal can be correctly decoded. This is one of the functions of the circuit based around one half of IC501.

IC501 is used as a Schmitt trigger feeds back either a high or low signal to indicate the presence of a RF signal to the system microprocessor, IC101. The threshold of the Schmitt trigger is controlled by the components fitted to pin 2 of IC501, which gives a level of 2.39V on pin 2 (inverting input). When the level on pin 3 (non-inverting input) reaches this level, pin 1 will change state. This change of state is detected by IC101 on pin 48 (AGC).

Audio Processing

In the current range of models fitted with the CA10 chassis there is the possibility of three different sound output types. These are mono, stereo (NICAM or AV) and SRS (Sound Retrieval System). The schematic diagram below shows the circuit arrangement for a typical SRS model.

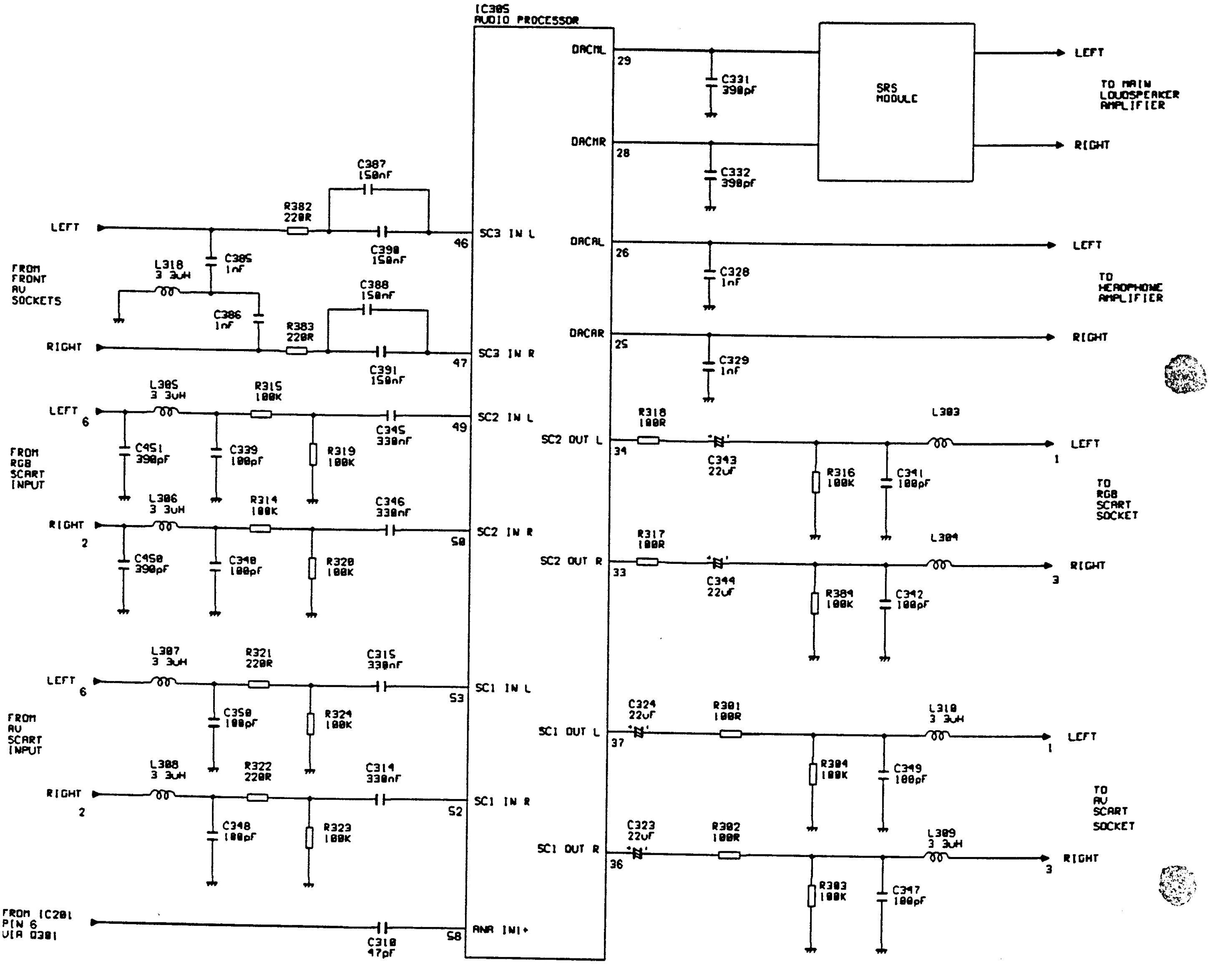
IC305
AUDIO PROCESSOR
DACML
29
DACMR
28
DACAL
26
DACAR
25
C331
390pF
C332
390pF
C328
1nF
C329
1nF
SRS
MODULE
LEFT
RIGHT
TO MAIN
LOUDSPEAKER
AMPLIFIER
LEFT
RIGHT
TO
HEADPHONE
AMPLIFIER
FROM
FRONT
AV
SOCKETS
LEFT
RIGHT
L318
3 3uH
C385
1nF
C386
1nF
R382
220R
R383
220R
C387
150nF
C390
150nF
C388
150nF
C391
150nF
SC3 IN L
46
SC3 IN R
47
FROM
RGB
SCART
INPUT
LEFT
6
RIGHT
2
L305
3 3uH
L306
3 3uH
C451
390pF
C450
390pF
C339
100pF
C340
100pF
R315
100K
R314
100K
R319
100K
R320
100K
C345
330nF
C346
330nF
SC2 IN L
49
SC2 IN R
50
SC2 OUT L
34
SC2 OUT R
33
R318
100R
R317
100R
C343
22uF
C344
22uF
R316
100K
R304
100K
C341
100pF
C342
100pF
L303
L304
LEFT
1
RIGHT
3
TO
RGB
SCART
SOCKET
FROM
AV
SCART
INPUT
LEFT
6
RIGHT
2
L307
3 3uH
L308
3 3uH
R321
220R
R322
220R
C350
100pF
C348
100pF
R324
100K
R323
100K
C315
330nF
C314
330nF
SC1 IN L
53
SC1 IN R
52
SC1 OUT L
37
SC1 OUT R
36
C324
22uF
C323
22uF
R301
100R
R302
100R
R304
100K
R303
100K
C349
100pF
C347
100pF
L310
3 3uH
L309
3 3uH
LEFT
1
RIGHT
3
TO
AV
SCART
SOCKET
FROM IC201
PIN 6
VIA Q301
C310
47pF
ANA IN1+
58

Figure 35 : Audio Stage Circuit Diagram

As can be seen from the diagram shown above, all the audio signal processing is undertaken by IC305 (MSP3410D). The MSP3410D is a Multi standards Sound Processor (MAP) that is capable of decoding and processing the majority of sound systems found around the world, depending on the instructions it receives on the I^2C bus. In this receiver it is set up for FM mono sound at 6MHz and NICAM stereo sound on 6.522MHz. Because of the programming of the memory this can not be changed, i.e. the receiver can not be modified for use in another country. It is possible to control a number of analogue audio inputs, this receiver is equipped with two SCART sockets (AV and RGB) on the rear and an AV socket on the front. These inputs can be switched to four outputs - rear AV and RGB sockets, headphones and main sound amplifier.

Control of IC305 is achieved over the I^2C bus 1 line. However control can only take place once the IC has been reset. Please refer to the **Resets and oscillators** section of these notes for more details on how IC305 is reset.

Note that SRS is provided on some models (51DS05H, 59DS05H and 66DS05H) and this system is described in more detail in the **Sound Retrieval System (SRS)** section of these notes.

Signal sources and generation

Audio signals come from four different sources, which are listed in the table below. Note that the IF input from the tuner is decoded within IC305 to produce the normal FM mono and stereo NICAM signals.

Signal Source	Left Source Pin	Right Source Pin	IC305 Left Input	IC305 Right Input
SCART	6	2	Pin 49, SC2 IN L	Pin 50, SC2 IN R
RGB	6	2	Pin 52, SC1 IN L	Pin 53, SC1 IN R
Front AV	Front AV sockets		Pin 46, SC3 IN L	Pin 47, SC3 IN R
Tuner (IF)	Pin 6 of IC201 (Video Out)		Pin 58, ANA IN1+	

RF audio signals are processed from the incoming sound IF signal on pin 58 of IC305. As can be seen from the **IF signals** section of these notes the incoming IF signal is split two ways, one goes to the video demodulator, the other to the sound stages. Once inside the IC, demodulation takes place of both the FM (mono) and NICAM (stereo) signals. Other signals come from the AV SCART, RGB SCART and front AV connectors. These are switched within the IC.

Signal switching

All audio signal switching is carried out within IC305 under control from the I^2C bus 2 line. The switching options are controlled from the video selection menu via the remote control or my direct switching by the SCART sockets.

Loudspeakers driver stage

Sound amplification and output is achieved by a discrete component output stage which is similar to that of the frame output stage (class D). This stage will be used in the first production of the CA10 chassis, however later chassis may be fitted with a single chip. No circuit description of this process will be given as at the time of preparing these notes, no final decision has be received from the factory.

Note that on this receiver there are three loudspeaker channels - left, right and sub-woofer.

Sound Retrieval System (SRS)

In the current range of models fitted with the CA10 chassis there is the option of three different types of sound output. These are mono, stereo (NICAM or AV) ans SRS (Sound Retrieval System). Dolby Pro-logic models are provided in the previous chassis range in the 59CSD8H and 66CSD8H which will continue to be produced alongside the CA10 models.

Normal stereo sound requires the listener to sit in the correct position to obtain the best advantage from the loudspeakers and that there is no apparent surround effect, i.e. no sound comes from behind the listener. Because of these shortcomings the SRS system was developed.

SRS changes the characteristics of the audio signal coming from the two stereo loudspeakers to give the effect of sound coming from a number of different directions at the same time. This is achieved by the use of phase shifting the signal and adding or reducing delays at certain frequencies. The overall effect is to give the signal a 'surround' feel. This is similar to the 'stereo wide' effect, but includes a depth that allows the listener to believe that the sound is coming from the sides as well.

As the SRS encoding process acts upon a conventional stereo signal, it is not necessary to encode the audio as with Dolby Pro Logic. Therefore this system will work with any stereo input, i.e. off air NICAM signal, from a stereo (Hi Fi) VCR or even a audio input via one of the SCART sockets.

Headphone driver stage

As the headphone volume can be controlled separately to that of the main loudspeaker output, i.e. it is possible to listen on headphones at a different sound level than that coming out of the loudspeakers, it is necessary to have a separate amplifier and control stage for the headphone socket. This is shown in the diagram below.

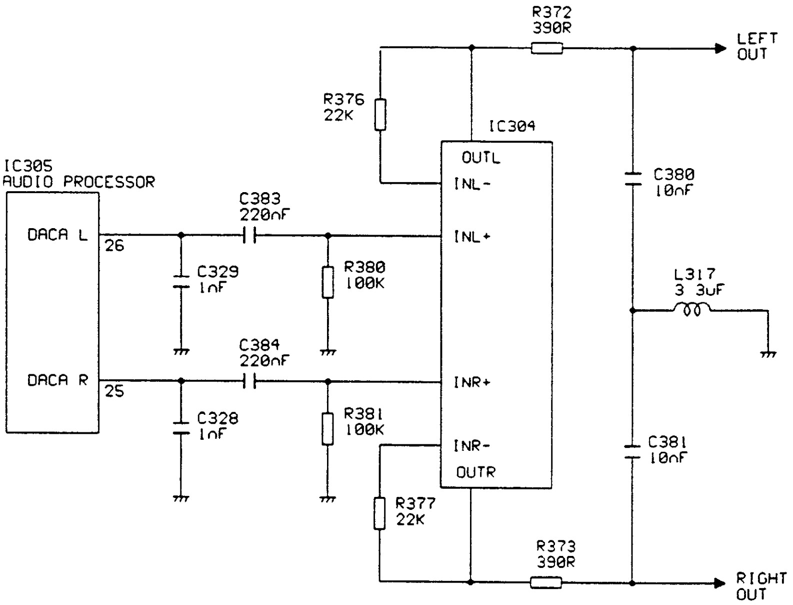

Figure 36 : Headphone Amplifier Circuit

The headphone amplifier is a conventional linear device that is supplied from the +18V supply off the chopper stage, it does not drawn enough current to justify a class D amplifier stage as is utilised in the speaker output circuit. Nominal headphone impedance is recommended to be 32 Ohms.

Video Processing

IC201 provides the majority of the signal processing functions and is controlled by the I^{2}C bus 1 line from the main system microprocessor, IC101. Video signal switching is carried out by IC401 which also provides Y and C inputs to IC201. Teletext, RGB and on screen display information are also fed into IC201, which then outputs these signals to the CRT drive amplifier, IC901.

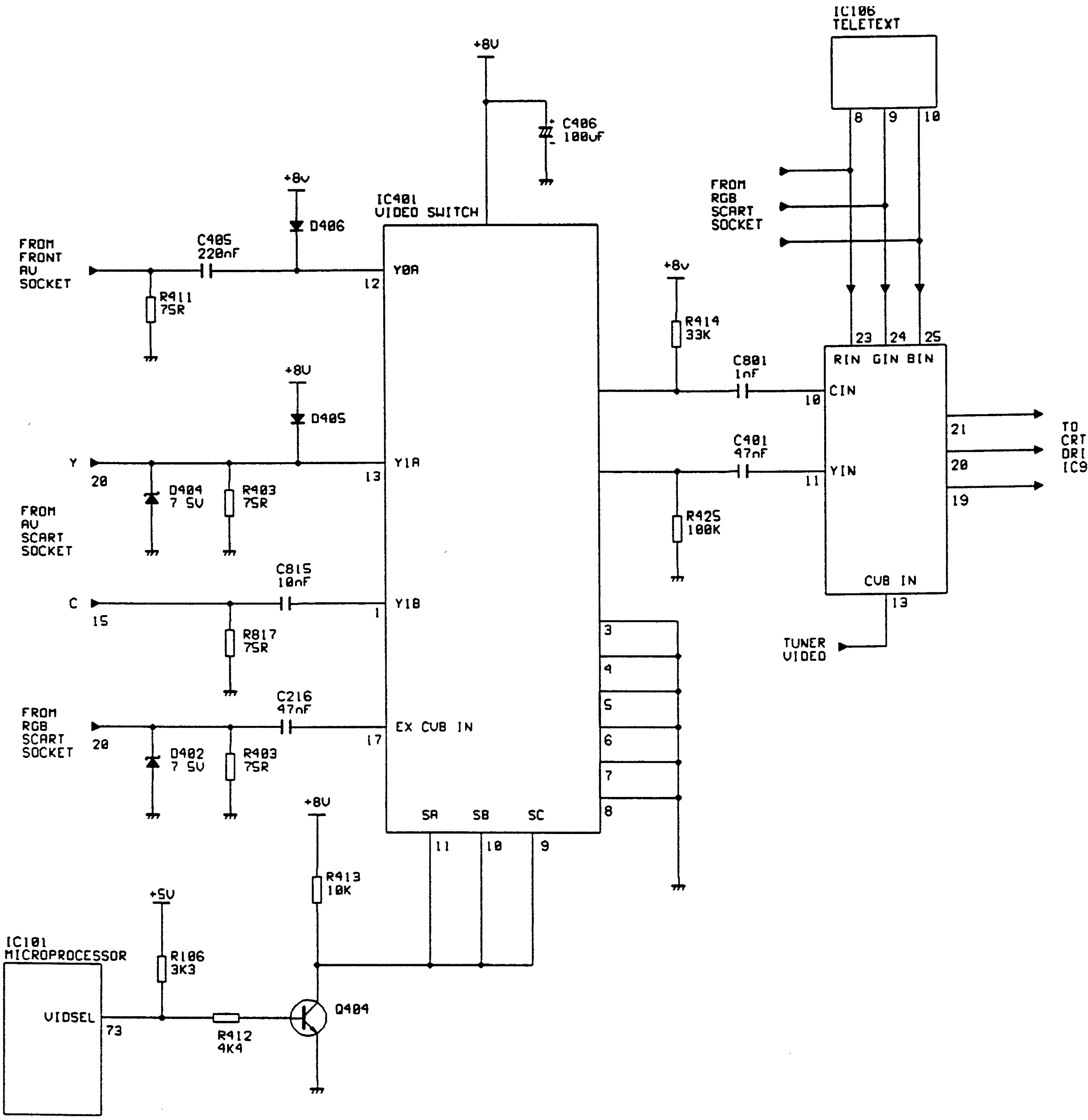
IC106
TELETEXT
8
9
10
+8V
C406
100uF
FROM
RGB
SCART
SOCKET
+8v
IC401
VIDEO SWITCH
D406
FROM
FRONT
AV
SOCKET
C405
220nF
12
Y0A
R411
75R
+8v
R414
33K
23
24
25
RIN GIN BIN
C801
1nF
10
CIN
+8V
D405
21
TO
CRT
DRIVE
IC901
C401
47nF
Y
20
Y1A
13
D404
7 5V
R403
75R
11
YIN
20
19
FROM
AV
SCART
SOCKET
R425
100K
C815
10nF
CVB IN
13
C
15
Y1B
1
3
R817
75R
TUNER
VIDEO
4
C216
47nF
5
FROM
RGB
SCART
SOCKET
20
EX CVB IN
17
6
D402
7 5V
R403
75R
7
+8V
SA
SB
SC
8
11
10
9
R413
10K
+5V
IC101
MICROPROCESSOR
R106
3K3
VIDSEL
73
R412
4K4
Q404

Figure 37 : Video Switching circuit diagram

The diagram above shows the video circuit in detail. Note that all inputs are terminated with a 75R load resistor to ensure correct impedance matching with the respective source. The SCART socket video inputs are protected from over voltage by the 7.5V zener diodes.

IC401 is a C-MOS triple 2 input analogue multiplexing IC. This means that depending on the switching signal applied to pins 9, 10 and 11 either pins 12 and 17 or 13 and 1 will be connected to pins 11 and 10 of IC201 respectively. IC201 is then controlled over the I^{2}C bus to take each input as a video source - as in the case of the front AV socket or RGB socket. In the case of S-VHS pin 13 of IC401 connects to pin 11 of IC201 and pin 1 to pin 10, IC201 is then instructed to processes these signals as S-VHS.

Signal sources and switching

Video signals can either be obtained from the tuner (RF channels from 20 to 69), front AV, rear S-VHS or the two SCART sockets located on the rear of the receiver - one of these is designated RGB. RGB signals also come from the teletext processor for text and for the on screen display, these are discussed further in the **Teletext**, **RGB switching** and **On screen display** sections of these notes. All these inputs are fed into IC201 (see table below), which switches to the required source under instruction from the main system microprocessor, IC101.

Source	Pin of Source	Pin of IC401	Pin of IC201
RGB Video	20	17	10
RGB	7/11/15	-	23/24/25
Tuner/IF	Pin 6 of IC201	-	13
Front AV	-	12	11
Teletext	IC106 8/9/10	-	23/24/25
OSD	IC106 8/9/10	-	23/24/25
SCART Y	20	13	11
SCART C	15	1	10

When the receiver is switched to the S-VHS input, it will select the rear AV SCART socket on pins 20 for luminance and 15 for chrominance and connects these to pins 11 and 10 of IC201 respectively.

RGB Switching

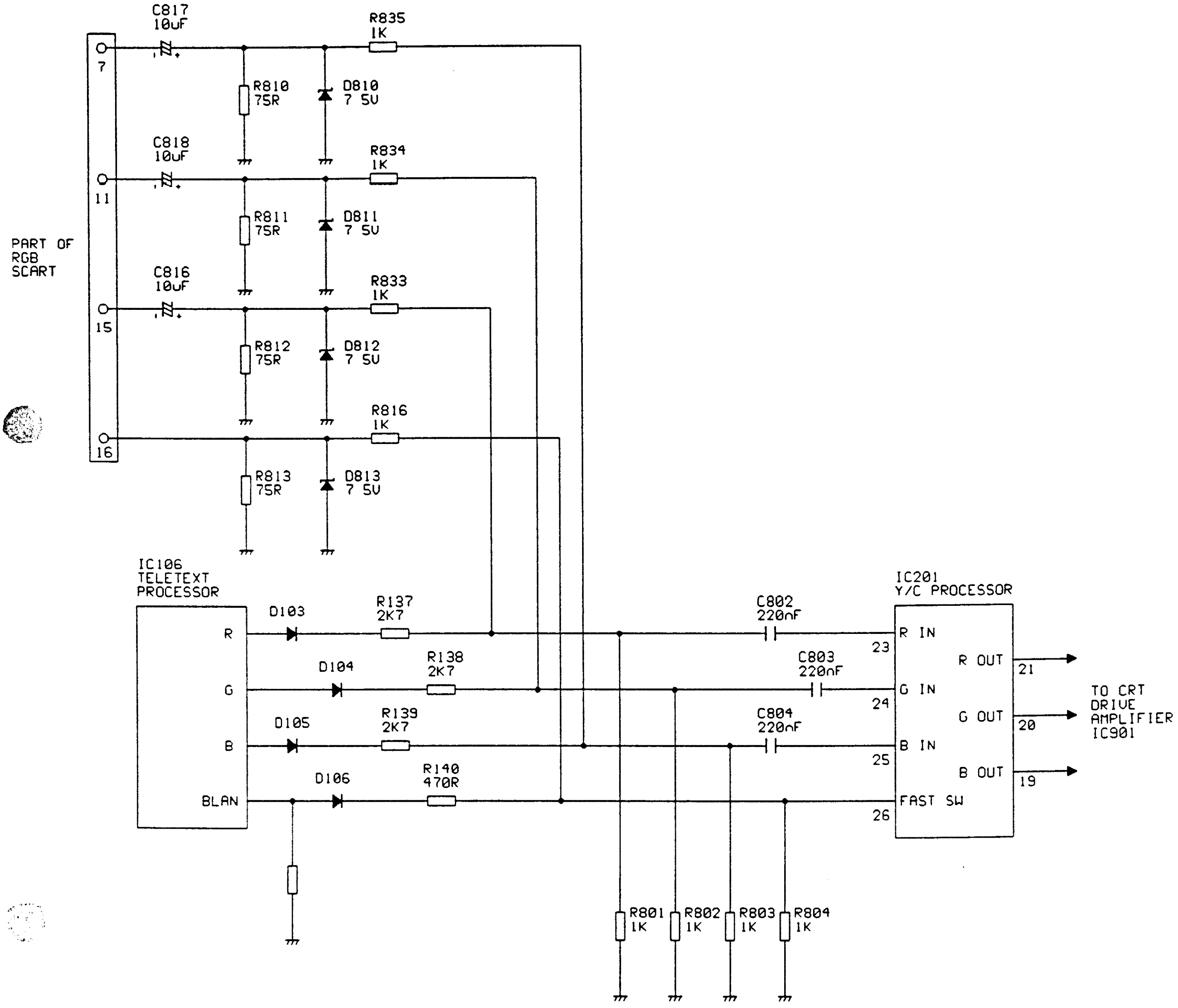
C817
10uF
R835
1K
7
R810
75R
D810
7 5V
C818
10uF
R834
1K
11
R811
75R
D811
7 5V
PART OF
RGB
SCART
C816
10uF
R833
1K
15
R812
75R
D812
7 5V
R816
1K
16
R813
75R
D813
7 5V
IC106
TELETEXT
PROCESSOR
R
G
B
BLAN
D103
R137
2K7
D104
R138
2K7
D105
R139
2K7
D106
R140
470R
C802
220nF
C803
220nF
C804
220nF
IC201
Y/C PROCESSOR
R IN
G IN
B IN
FAST SW
23
24
25
26
R OUT
G OUT
B OUT
21
20
19
TO CRT
DRIVE
AMPLIFIER
IC901
R801
1K
R802
1K
R803
1K
R804
1K

Figure 38 : RGB Input and Switching Circuit

It is possible to feed in a RGB signal (computer, games console, etc.) to this receiver via the RGB SCART socket located on the rear of the receiver. Switching for this input is either via direct selection on the remote control or by automatic switching using the fast switching pin on the socket, pin 16.

D103/4/5/6 prevent IC106 loading any of the input signals should they be present and D810/11/12/13 prevent any large voltage spikes that may appear on the inputs from damaging IC201. R810/11/12/13 are for impedance matching. Note that each signal input is coupled via a 10uF capacitor (C816/7/8) this is to ensure that the signals do not contain a dc level which may upset the processing stages. The fast switch input is DC coupled as this will be a voltage level used to switch IC201 to this input.

IC201 internally generates a RGB signal from the incoming video, this RGB signal and that generated by the RGB socket/teletext IC/on screen display are then switched internally to feed into IC901 to drive the CRT.

Teletext

Teletext processing is carried out within IC106 (STV5346). This IC is a 28 pin dual in line flat pack that contains all the normal fast text processing capabilities including a small page store and on screen display generation.

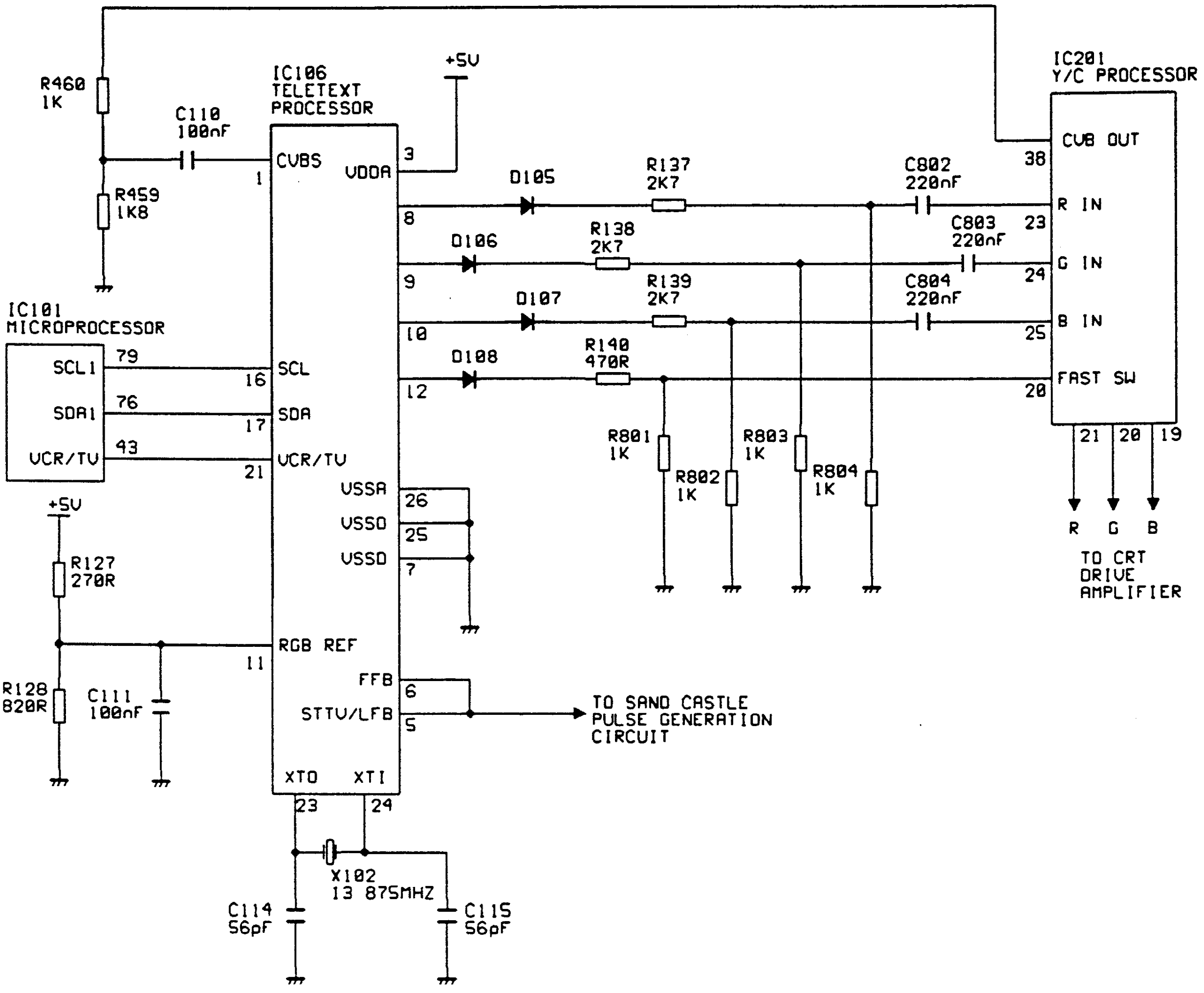
IC106
TELETEXT
PROCESSOR
IC201
Y/C PROCESSOR
IC101
MICROPROCESSOR
R460 1K
R459 1K8
C110 100nF
CVBS
VDDA
+5V
D105
D106
D107
D108
R137 2K7
R138 2K7
R139 2K7
R140 470R
C802 220nF
C803 220nF
C804 220nF
CVB OUT
R IN
G IN
B IN
FAST SW
SCL1
SDA1
VCR/TV
SCL
SDA
VSSA
VSSD
RGB REF
FFB
STTV/LFB
XTO
XTI
R801 1K
R802 1K
R803 1K
R804 1K
R127 270R
R128 820R
C111 100nF
X102
13 875MHZ
C114 56pF
C115 56pF
R G B
TO CRT
DRIVE
AMPLIFIER
TO SAND CASTLE
PULSE GENERATION
CIRCUIT

Figure 39 : Teletext Processor Circuit

When the user selects the teletext function, IC101 instructs the teletext processor, via the I²C bus 2 line, to switch IC201 to the RGB input via pin 12 of IC106. Any RGB signals coming out of IC106 will now be switched by IC201 to the CRT drive amplifier, IC901.

As the teletext encoded information is contained within the incoming video signal, it is necessary to ensure that the teletext processor is supplied with a composite video input. This composite signal enters IC106 on pin 1 (CVBS). Decoding takes place within the IC, using the clock frequency of 13.873MHz generated by X102.

On screen display

Graphics that appear on the screen during the various control functions (Sound control, picture adjustments, tuning settings, etc.) are all generated within IC106 under control from the main system processor. The information used to generate the characters themselves is contained within the EPROM, IC105. This data is dependant upon the control codes programmed within the microprocessor, IC101 at manufacture, i.e. language, receiver functions etc. Therefore the microprocessor is dependent on the destination country. Note that if this information is corrupted, then the receiver may start up in the incorrect language or have a corrupted character set. It is very unlikely that the EPROM, IC105 would fail in this way.

CRT drive circuit

Drive for the CRT cathodes is provided on the CRT base panel. Most of the amplification is carried out within one IC, IC901 (TDA6107Q). To enable IC901 to work correctly it requires a supply of 150V, which is taken from the main HT off the chopper power supply.

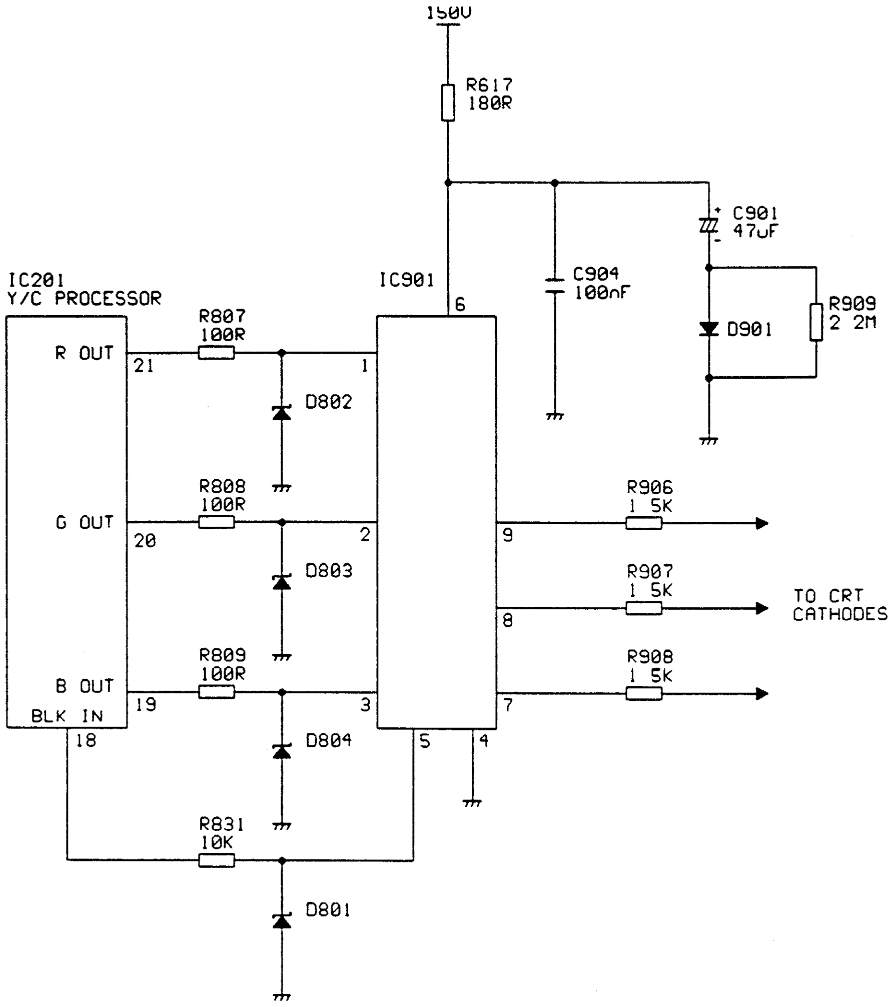
150V
R617
180R
C901
47uF
C904
100nF
R909
2 2M
D901
IC201
Y/C PROCESSOR
R OUT
G OUT
B OUT
BLK IN
21
20
19
18
R807
100R
R808
100R
R809
100R
R831
10K
D802
D803
D804
D801
IC901
1
2
3
4
5
6
7
8
9
R906
1 5K
R907
1 5K
R908
1 5K
TO CRT
CATHODES

Figure 40 : CRT Drive Amplifier Circuit

From the Y/C processor, IC201, the RGB drive signals connect to IC901 via feed resistors and spike suppression zener diodes which ensure that any excessive drive variations do not damage the IC. The outputs from IC901 drive the CRT cathodes directly via the 1.5k current limiting resistors.

Black level clamping is derived during the frame blanking period, a DC level is supplied by monitoring the earth return current from the internal drive FET's during this time.

Indicating Devices

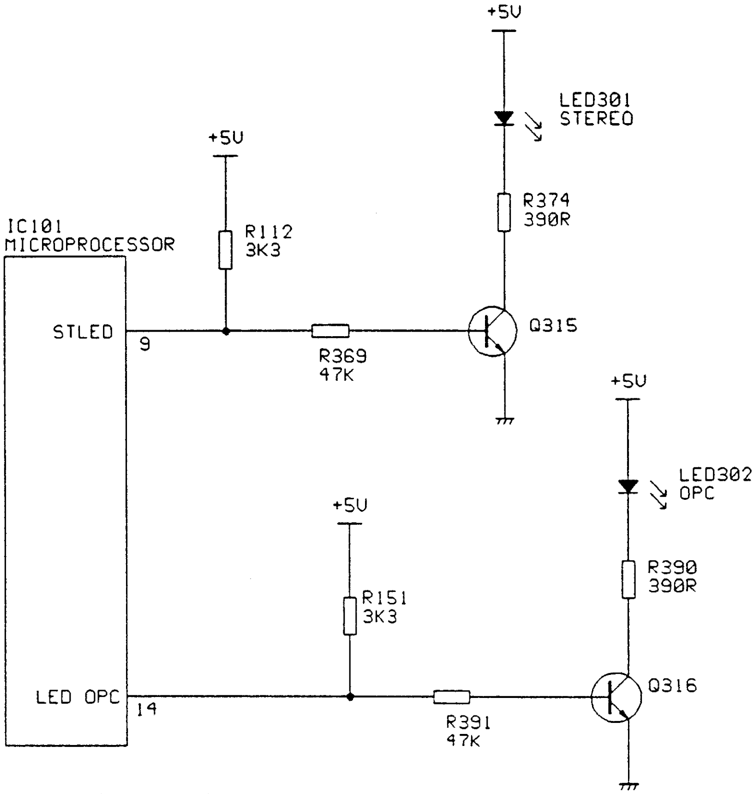
+5V
LED301
STEREO
+5V
R374
390R
IC101
MICROPROCESSOR
R112
3K3
STLED
9
R369
47K
Q315
+5V
LED302
OPC
+5V
R390
390R
R151
3K3
LED OPC
14
R391
47K
Q316

Figure 41 : Stereo and OPC LED Drive Circuit

There are three indicating devices used within the CA10 chassis. The first of these is the standby indicator, which is a neon connected across the live and neutral mains input, after the mains switch. This will illuminate whenever mains is applied to the set.

The second indicator is the stereo LED. Whenever a stereo broadcast is being received (a NICAM signal is being decoded), the audio processor will communicate with the system control microprocessor over the I^2C bus 1 line and instruct it to give a high on pin 9 (STLED) so that LED301 illuminates. Note that when a stereo input is fed into the receiver via one of the SCART inputs or the front AV input, the stereo LED will not illuminate.

Thirdly there is the OPC indicator. This LED, LED302 is turned on by a high level on pin 14 (LEDOPC) of IC101. The OPC function is turned on and off by selection of the picture menu via the remote control.

Practical Fault Finding

I²C bus line disconnection

It is possible to isolate the various devices controlled by the I²C line by removing the feed resistors. A different symptom will be apparent depending upon which device is isolated as described below.

Tuner

If the tuner is isolated from the I²C bus line by removing resistors R201 and R202, all functions will work correctly except that there will be no picture, i.e. there will be no output from the tuner and a snowy raster will appear. This will continue until the blue mute operates

IC201 (IF, Y/C processor and time base generator)

IC201 can be isolated from the I²C bus by disconnecting resistors R232 and R233. When the set is turned on, the power supply will run, but there will be no raster. The NICAM LED will flash on/off at a 50% duty cycle once every second.

IC305 (Sound processor)

When IC305 is isolated from the I²C bus by removing R307 and R308, the picture and OSD operation will work correctly, but there will be no sound.

SRS module

If the SRS module is disconnected from the communication lines, by pulling out the sub panel, then there is no sound but the set continues to function normally.

Shorting of SDA to SCL

If the clock and data lines are shorted together, then the line and frame stages do not start up, although the power supply is active and the NICAM LED flashes on/off at a 50% duty cycle once every second.

Disconnection of IC703

IC703 provides communication to the primary microprocessor and if it is removed from the circuit all circuit functions will work correctly except that the set can not be brought out of standby with the use of the front buttons.

Power supply voltage line resistances to earth

Some times it is necessary to ensure that the supply lines are not loading the power supply unnecessarily. To this end it is useful to have an approximate static resistance of each supply. Typical readings are shown below.

Measured Voltage	Measuring Point	Resistance	Pin of T701
+18.1V	Cathode of D718	=>1k	8
-18.0V	Anode of D719	=>1k	3
+149.7V	Cathode of D720	=>50k	4
+10.2V	Cathode of D721	=>5k	5
+7.1V	Cathode of D722	=>450R	1
8.0V	Output of IC706	=>5k	-
5.0V	Emitter of Q706	1.25k	-
5.0V	Emitter of Q707	800R	-

Service Set Up Mode

To enable the engineer to correctly set up and adjust this chassis, it is possible to enter the service mode as described below.

Access and operation

To access the service mode

1. Turn the mains supply off.
2. Press the volume down and channel up button simultaneously.
3. Turn the mains supply on while still holding down the two buttons.
4. Keep the two buttons pressed until the picture appears.
5. Release the two buttons and the receiver is now in the service mode.

Adjustments

Adjustments are made using the channel up and down buttons to choose the adjustment to be made and then the volume buttons to change the value.

To store the adjustment, press the standby button.

Vertical adjustments

Vertical slope
S correction (59 and 66cm versions only)
Vertical shift
Vertical amplitude

Line

East/west width (59 and 66cm versions only)
Horizontal shift
East/west parabola (59 and 66cm versions only)
East/west width (59 and 66cm versions only)
East/west trapezoid (59 and 66cm versions only)
East/west corner (59 and 66cm versions only)

Introduction to the CA1 Chassis

As the CA10 chassis is designed for use as a NICAM and fast text unit, it is not suitable to be used in the small screen models that only feature basic functions. For this reason, the Sharp development engineers at the Spanish factory, located in Barcelona, have designed a small screen chassis, this is designated the CA1.

Use is made of a relatively standard chip set as outlined below :-

> **IC201** (TDA8840) - this is the main Y/C processing and time base generator IC that also contains all of the IF (audio and video) and audio analogue processing circuit (except for audio output).
>
> **IC1001** - this is the main processor unit that controls the functionality of the receiver. It is a masked device and therefore must be replaced with the correct type from the Sharp Spare Parts Centre if it fails. Note that within the teletext versions of the CA1 chassis this IC will contain the teletext processor.
>
> **IC1002** - is the non volatile memory that contains all the pre-set information for this receiver. It is important that the correct part number is used when obtaining a replacement device.

Although similar in many respects to the CA10, there are a number of important differences as indicated in the list below :-

1. The chopper power supply circuit is virtually the same as the CA10, but the component references are different. The voltage regulation circuit on the isolated side of the power supply is simpler and is covered in the **CA1 Power Supply** section.
2. No class D amplifiers are used, instead discrete component linear amplifiers have been used for both the vertical and sound output stages and are described in detail later in these notes. Note that the vertical output stage has been used in many previous Sharp small screen models.
3. Data communication is simpler, as only one I^2C bus is used and there is no external EEPROM as the microprocessor has this fitted internally (masked processor). To reduce the component count even further on the teletext models, the teletext processing action is also contained within the microprocessor.
4. As the power supply is kept running in this chassis, it is necessary to switch some of the secondary supplies, this is covered in the **CA1 Power On Control** section
5. A more sophisticated protection circuit is connected to the main processor. This is discussed in the **CA1 Protection** section.
6. The line driver circuit is different, and is described in the **CA1 Line Stage** section.

Note that the CA1 chassis section of these notes are based upon the 37DM23H service manual (part number SELH37DM23H//). This service manual is available from Teega Agencies, telephone number 01282 419917.

CA1 Receiver Specifications

Features	37DM23H	37DT25H	51DT25H
Tube Size (inches)	14	14	21
Visible Screen (cm)	34	34	51
Tube Type	Tinted	Tinted	B Matrix
Number of Pre-sets	99	99	99
Fast Text	No	Yes	Yes
On/Off Timer	Yes	Yes	Yes
Rear S-VHS Input	-	-	Yes
21 Pin Euroscart	1	1	1
Power Output (MPO)	2	2	4
Headphone Jack	Yes	Yes	-
Stand	No	No	Yes
Width (mm)	366	366	539
Height (mm)	325	325	468
Depth (mm)	375	375	484
S/B Power	9.5W	9.5W	9.5W

Notes :

Sharp reserve the right to make design and specification changes for product improvement.

The performance specification figures are nominal values of production units. There may be some deviation from these figures in individual units.

Block Diagram of the CA1 Chassis

A block diagram of the CA1 chassis is shown below. It can be clearly seen from this that the sound processing and teletext IC's have been deleted. All audio decoding is carried out within IC201 and the teletext function (37DT25H and 51DT25H) is carried out by the masked microprocessor (IC1001).

Unlike the CA10, the power supply is kept running in the standby mode and it is only the secondary voltages that are controlled to bring the receiver out of standby.

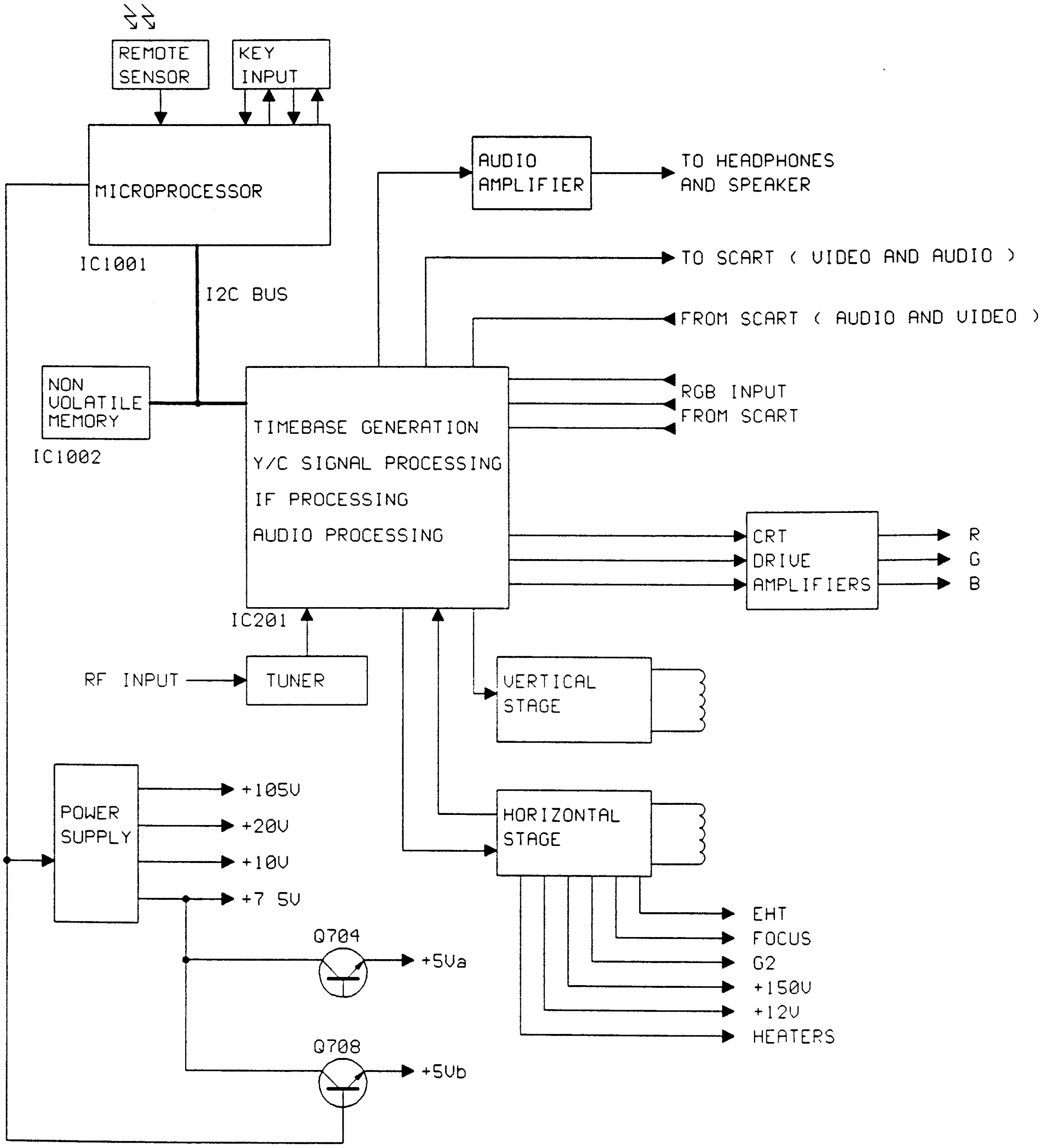
REMOTE SENSOR
KEY INPUT
MICROPROCESSOR
IC1001
I2C BUS
AUDIO AMPLIFIER
TO HEADPHONES AND SPEAKER
TO SCART (VIDEO AND AUDIO)
FROM SCART (AUDIO AND VIDEO)
NON VOLATILE MEMORY
IC1002
TIMEBASE GENERATION
Y/C SIGNAL PROCESSING
IF PROCESSING
AUDIO PROCESSING
IC201
RGB INPUT FROM SCART
CRT DRIVE AMPLIFIERS
R
G
B
RF INPUT
TUNER
VERTICAL STAGE
HORIZONTAL STAGE
POWER SUPPLY
+105V
+20V
+10V
+7 5V
Q704
+5Va
Q708
+5Vb
EHT
FOCUS
G2
+150V
+12V
HEATERS

Figure 42 : Overall Block Diagram of the CA1 Chassis

CA1 Power Supply

The power supply used in the CA1 chassis is very similar to that used in the CA10, except that its current suppling characteristics are lower and it does not turn off while the receiver is in standby. Therefore IC702 is not fitted and the power consumption of this receiver will be higher than that of the CA10, at approximately 9.5W. Note that on the actual circuit, some of the component references will be different, but the circuit configuration and operation remains the same. Please refer to the beginning of these notes for more information.

The following voltages are generated by the chopper stage. Note that the +5Va line is always present and that the +105V supply is regulated in standby, i.e. it will measure +105V in standby.

Stand by Voltage	Running Voltage	Resistance to Ground	Generation Point
+20.1V	+20.3V	=<100k	D719 cathode, Pin 16 of T700
+105.8V	+104.3V	=<80k	D708 cathode, Pin 11 of T700
+9.4V	+9,8V	=<100k	D709 cathode, Pin 12 of T700
-11.3V	-11.6V	=<100k	D710 anode, Pin 14 of T700
+7.0V	+7.1V	=<20k	D712 cathode, Pin 9 of T700
0V	+5.1V	1.4k	Q708 emitter
+5.1V	+5.1V	Approx 500R	Q704 emitter

As the load on the power supply is increased, the frequency of operation will decrease, conversely, as the load on the power supply decreases, the frequency of operation increases. While in the running mode, the frequency of operation is approximately 100kHz, which is obviously dependent on a number of factors, the main ones being beam current and volume setting. Whilst in standby the frequency is about 160kHz.

Regulation Control Circuit

As mentioned previously, the basic construction and operation of the power supply circuit is similar to that of the CA10 chassis. However, the major difference is the voltage fed back circuit which is shown in the diagram below.

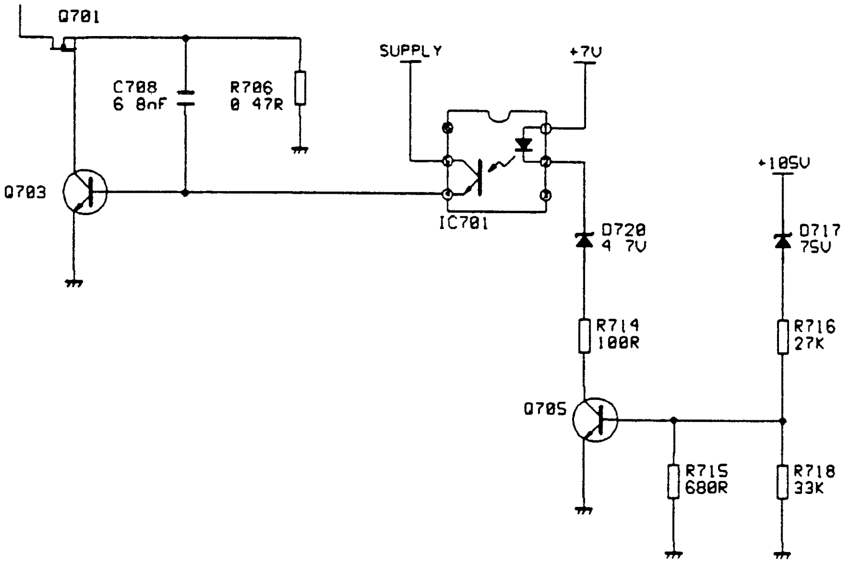

Figure 43 : CA1 Voltage Regulation Feed Back Circuit

It can be seen that the +105V supply is monitored using a potential divider network that feeds straight into the base of a control transistor. The collector of this transistor will affect the brightness of the LED inside the opto coupler and hence the conduction of the photo transistor. Regulation is achieved by varying the on time of the chopper transistor.

If the main supply were to rise, the voltage on the base of Q705 will also rise, turning it on harder. The brightness of the LED would increase as the voltage on pin 2 of the opto coupler drops. In turn, this allows the transistor to conduct harder and hold on Q703 for longer, turning off Q701 for longer and thus reduce the supply.

If the main supply were to fall, the voltage on the base of Q705 will also fall, reducing its conduction. The brightness of the LED would decrease as the voltage on pin 2 of the opto coupler rises. In turn, this allows the transistor to turn off sooner and hold on Q703 for a shorter period, turning off Q701 for a shorter period and thus increase the supply.

IC201 Supply

It was found that the power feed circuit for IC201 as used in the CS chassis would sometimes fail and cause IC201 to work erratically. To alleviate this problem, a new regulation circuit has been designed to provide the +8V supply to pin 53 of IC201. This circuit is shown below.

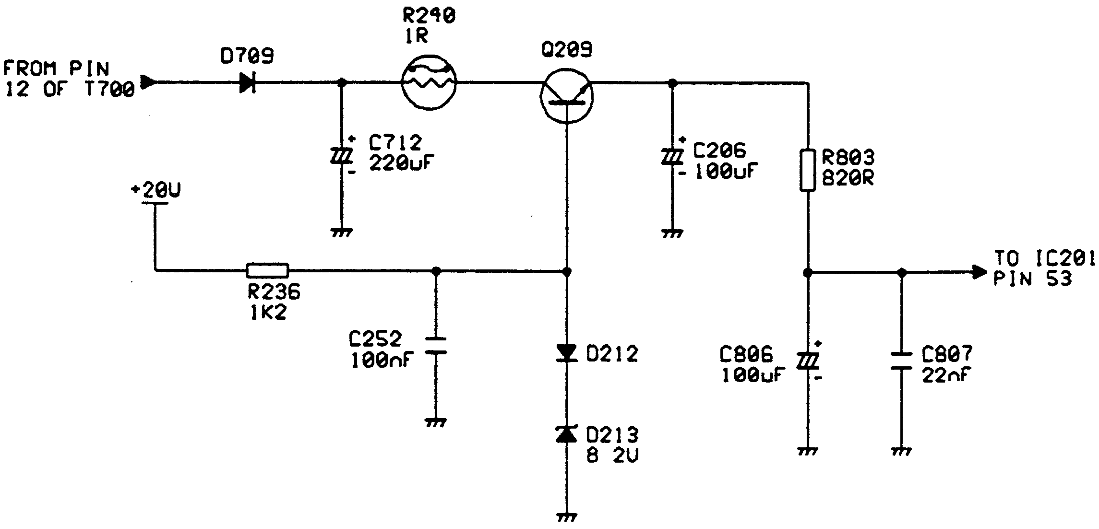

Figure 44 : IC201 Power Supply Circuit

Q209 is a simple series regulator, whose emitter voltage is dependant upon D212 and D213. The actual measured voltage the emitter of Q209 is +8.2V (D213 voltage - D212 voltage + Q209 base/emitter volt drop). Note that the biasing for D212 and D213 is taken from the +20V supply. This will ensure that if there is a failure with either the +10V or +20V supplies, IC201 will not generate any vertical or horizontal drive signals.

D709 also provides the +10V rail that is used by the vertical stage.

CA1 Reset

Whenever the receiver is switched on from the mains (on/off button pressed) it is necessary to reset the main microprocessor, IC1001. This process is achieved with the use of the circuit outlined below.

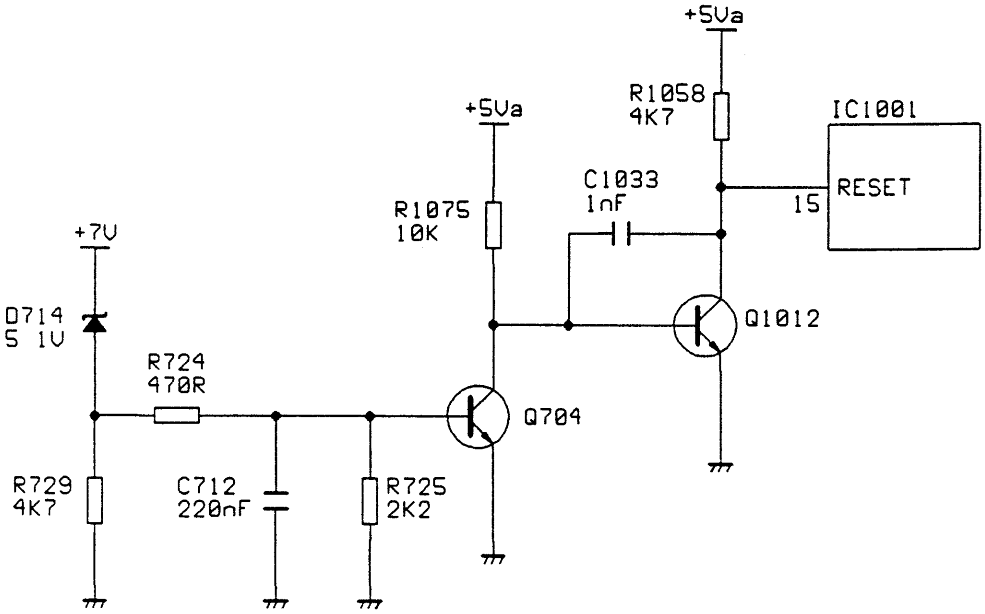

Figure 45 : CA1 Reset Circuit

When the power supply starts up, a permanent +5V line , designated +5Va, will be generated via D712 and series regulator Q704. This supply, along with that produced by D712 (+7V), is used to produce the reset pulse that is fed to pin 15 of IC1001.

At start up D714 (a 5.1 volt zener diode) will start to conduct when the +7V supply reaches 5.1V, allowing the +5Va line to come up and supply the microprocessor, IC1001. This will allow C712 to charge via R724. When this voltage rises to 0.65V, Q704 will turn on and its collector voltage will drop, which in turn will turn off Q1012 allowing its collector to rise. IC1001 is now reset.

R725 will discharge C712 quickly should the set be turned off then on again quickly, thus preventing corruption of the reset pulse and possibly IC1001 hanging. Capacitor C1033 will sped up the switching action of Q1012.

Data Communication

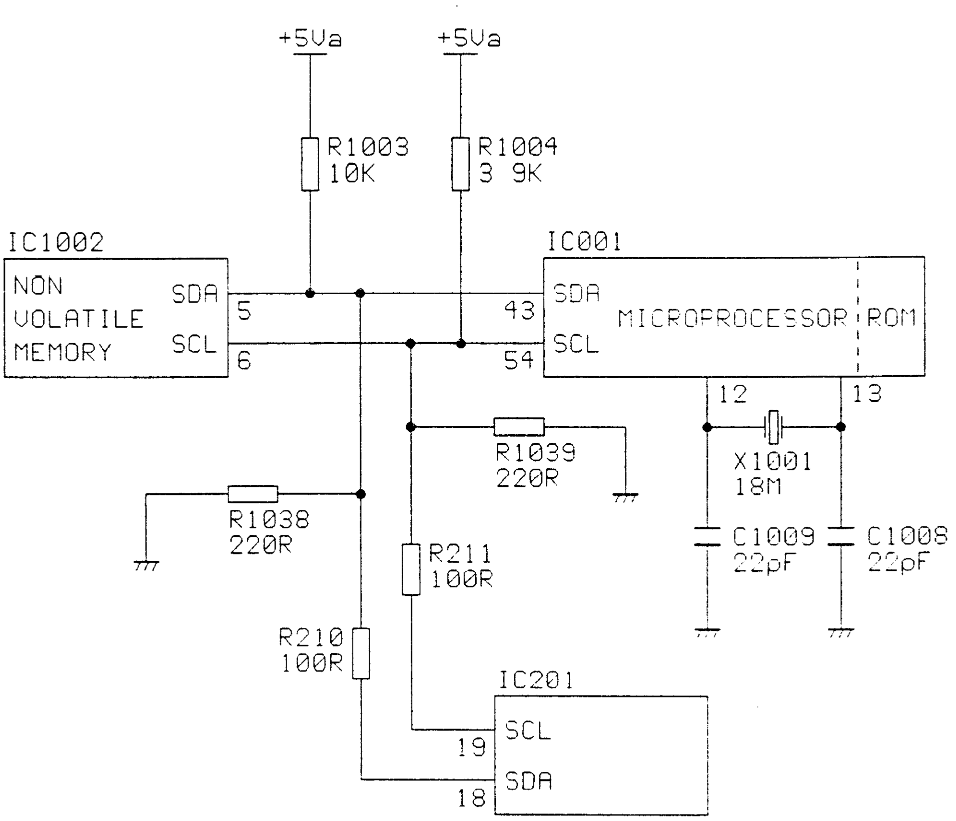
+5Va
+5Va
R1003
10K
R1004
3 9K
IC1002
NON
VOLATILE
MEMORY
SDA
SCL
5
6
IC001
SDA
SCL
43
54
MICROPROCESSOR
ROM
12
13
X1001
18M
C1009
22pF
C1008
22pF
R1039
220R
R1038
220R
R211
100R
R210
100R
IC201
SCL
SDA
19
18

Figure 46 : CA1 Data Communication

To enable the receiver to work correctly it is necessary to provide some form of communication between the microprocessor and the NVM and IC201. This is provided by a single I^{2}C bus from pins 43 (SDA) and 54 (SCL) of IC1001. This configuration is considerably simpler than that of the CA10 chassis.

A clock is provided at 18MHz to control the internal processing of IC1001. If this clock stops, then the receiver will not work (dead).

IC1001 is divided up into a number of processing sections, one of these will contain the ROM that instructs the microprocessor. Therefore, it is important to order the correct microprocessor if it should fail. For example, a microprocessor fitted to a 37DM23H will not work in the text version of this set, the 37ST25H.

CA1 Power On Control

During the stand by mode, IC1001 (main microprocessor) is supplied with the standby +5Va from the chopper stage on pins 11 and 37. This supply is generated by the series regulator transistor Q704 from the supply generated by D712 off pin 9 of T700.

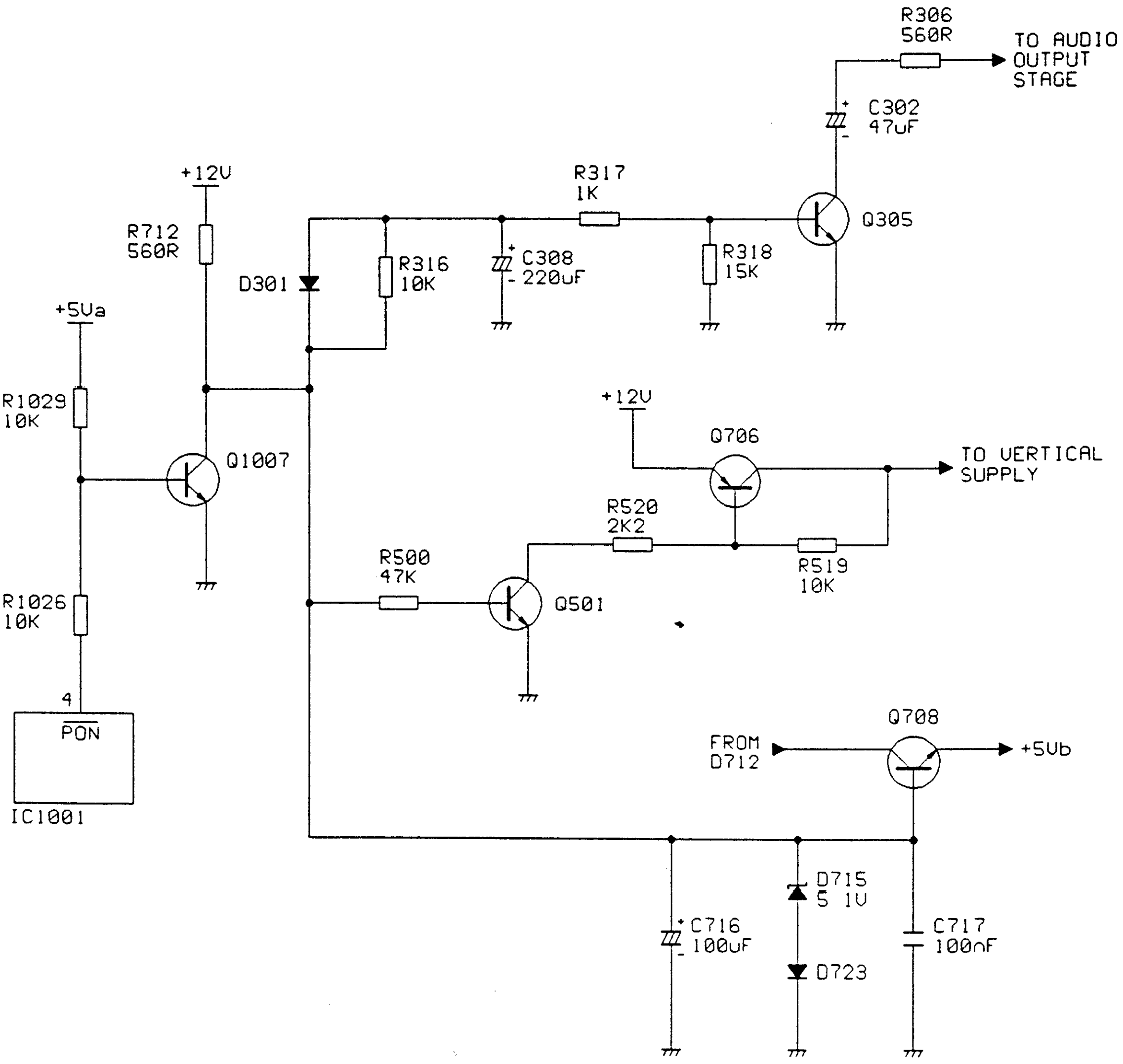
R306
560R
TO AUDIO OUTPUT STAGE
C302
47uF
+12V
R317
1K
Q305
R712
560R
R316
10K
C308
220uF
R318
15K
D301
+5Va
R1029
10K
Q1007
+12V
Q706
TO VERTICAL SUPPLY
R520
2K2
R519
10K
R500
47K
Q501
R1026
10K
4
PON
IC1001
Q708
FROM D712
+5Vb
D715
5 1V
C716
100uF
C717
100nF
D723

Figure 47 : CA1 Power On Control Circuit

To enable the set to turn on, pin 4 of IC1001 goes low, which turns off Q1007 and allows its collector voltage to rise up to 5.7V (set by the shunt regulator comprising of R712, D715 and D723). Series regulator Q708 turns on and provides the +5Vb running supply. At the same time Q501 is turned on and Q706 also, this provides the +10V supply to the frame output stage. Once these supplies have come up, the microprocessor will allow the line, then frame stages to start up.

A feed from the collector is also taken to the base of Q305 via R316 and C308, this is to prevent any sound from emanating from the loudspeakers during start up. C302 and R306 will drag down the audio signal momentarily as the charge on C308 builds up. This muting action will only last a few seconds. Note that when the set is taken back into standby, D301 will rapidly discharge C308 so if the receiver is turned on again quickly, the same action will take place.

CA1 Protection

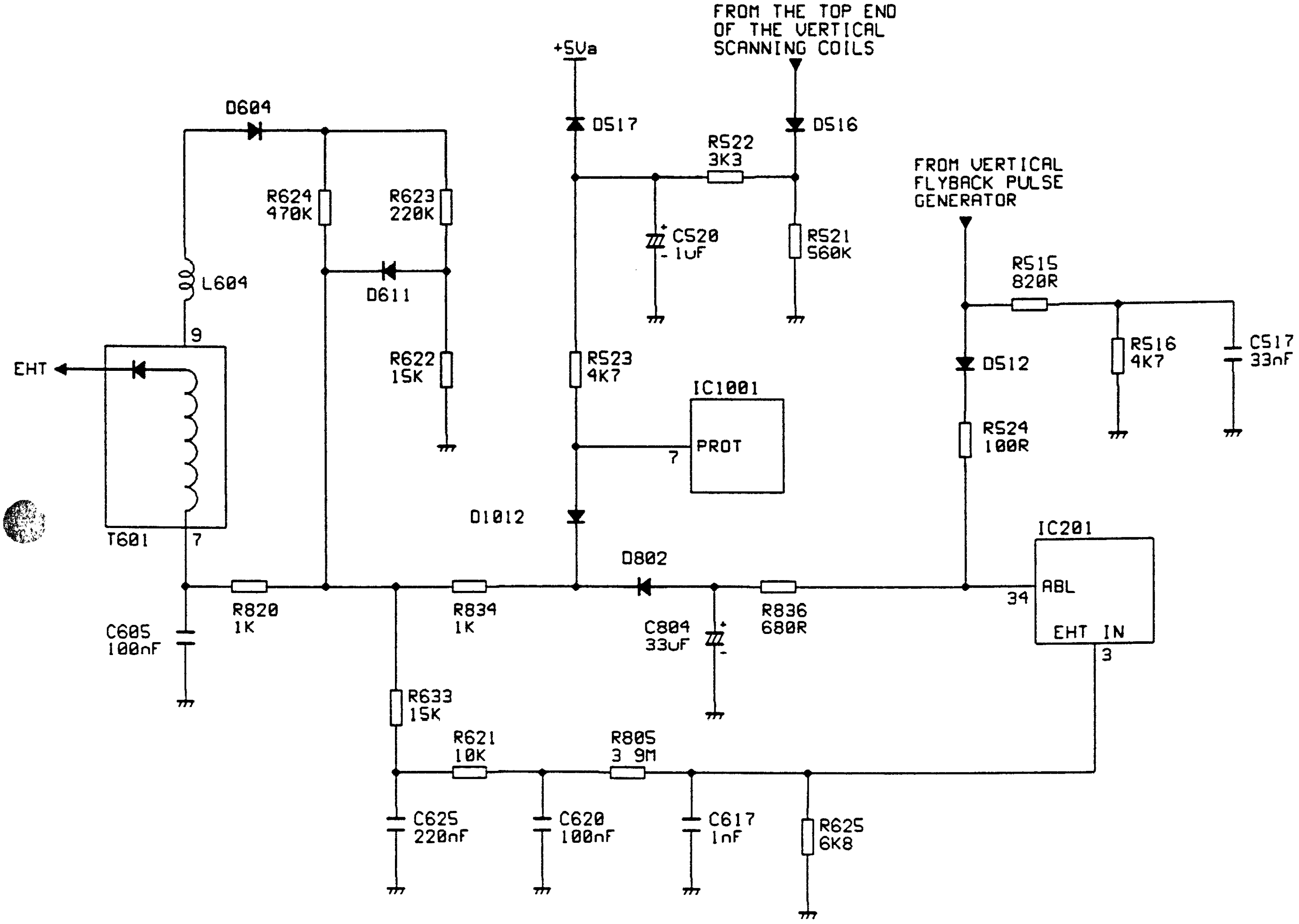
FROM THE TOP END OF THE VERTICAL SCANNING COILS
+5Va
D604
D517
D516
R522 3K3
FROM VERTICAL FLYBACK PULSE GENERATOR
R624 470K
R623 220K
C520 1uF
R521 560K
L604
D611
R515 820R
9
EHT
R622 15K
R523 4K7
IC1001
PROT
7
D512
R516 4K7
C517 33nF
R524 100R
D1012
IC201
T601
7
D802
ABL
34
EHT IN
3
R820 1K
R834 1K
C804 33uF
R836 680R
C605 100nF
R633 15K
R621 10K
R805 3 9M
C625 220nF
C620 100nF
C617 1nF
R625 6K8

Figure 48 : CA1 Protection Circuit

Unlike the CA10 chassis, the CA1 incorporates a protection circuit that operates with inputs from the beam current limiter, frame output stage and CRT drive amplifier supply.

Basic protection is provided should the frame drive or beam current feed back drop below 1.5V on pin 7 of IC1001 (PROT). Should this happen, then it is possible to over ride the protection circuit by removing D1012 from the circuit, this will allow pin 7 to rise up to +5V via R1066. Note that the nominal state of pin 7 is +5V.

Automatic Beam Current Limiting and X-Ray Protection

Pin 34 of IC201 (ABL) serves the same function as in the CA10 chassis, which is to blank the screen should there be excessive beam current or a frame scan problem. If the beam current increases too far, an ultra black picture will be produced by reducing the black level of the video signal to sync level.

From the vertical stage, the flyback pulse is also monitored so that in the event of a frame collapse or a malfunction in the scanning coil drive circuit, the CRT emission will be blanked. This is desirable to reduce the risk of damage to the CRT phosphors.

If the beam current continues to increase, there will be a danger of forward X-ray emissions from the CRT face. This is avoided by monitoring the voltage level on pin 3 (EHT IN) of IC201 and should this rise above a pre-defined level, the receiver will shut down.

CA1 Discrete Component Vertical Stage

Unlike the CA10 chassis, the vertical output stage used in the CA1 chassis is a discrete component type circuit. The circuit descriptions below explain the function and operation of the vertical driver and output stages. Note that a very similar circuits are used in previous ranges of Sharp small screen television receivers.

Vertical Driver Stage

IC201 generates the vertical drive and geometry correction signals (geometry settings contained within the non volatile memory, IC1002). The circuit shown below is the driver stage for the output stage.

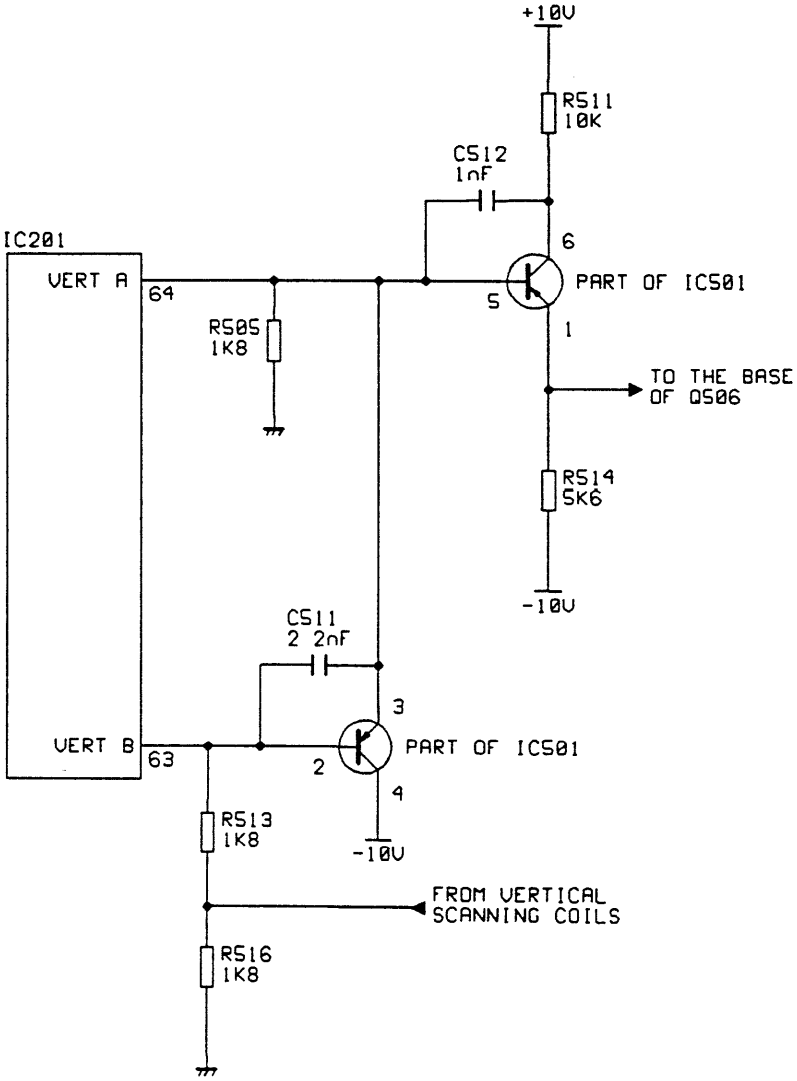
+10V
R511
10K
C512
1nF
IC201
VERT A
64
6
PART OF IC501
5
R505
1K8
1
TO THE BASE OF Q506
R514
5K6
-10V
C511
2 2nF
3
VERT B
63
PART OF IC501
2
4
R513
1K8
-10V
FROM VERTICAL SCANNING COILS
R516
1K8

Figure 49 : CA1 Vertical Driver Stage

From pin 64 of IC201, the main drive signal enters the base of the driver transistor (top of circuit). At the same time, the correction signal from pin 63 and feedback from the output stage is added to the driver base via the bottom transistor. The two transistors are housed in the same package to give stable operation within a wide temperature range.

As the top transistor is used as a emitter follower, its emitter signal will closely follow the base.

Vertical Output Stage

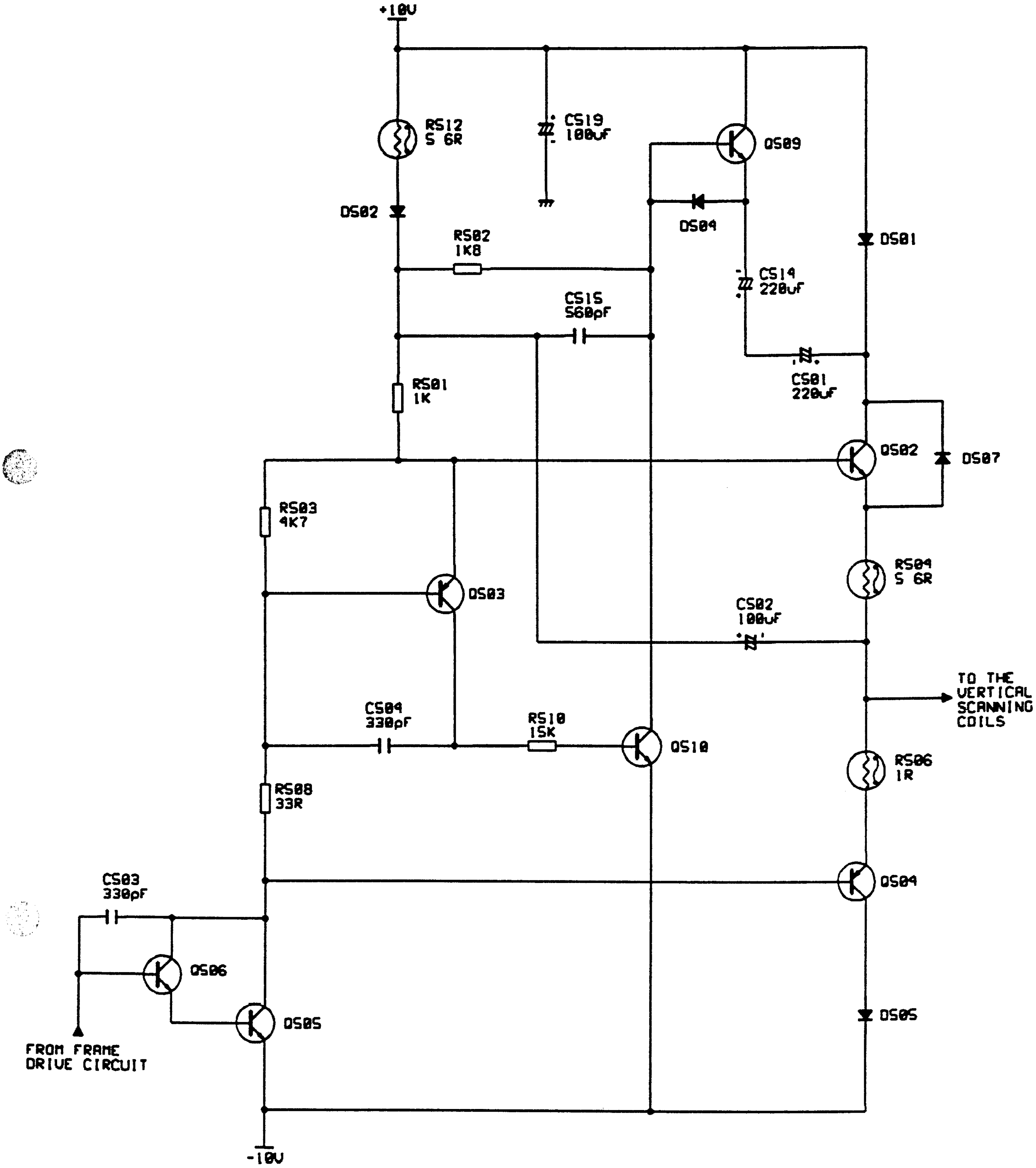
+10V
R512
5 6R
C519
100uF
Q509
D502
R502
1K8
D504
D501
C514
220uF
C515
560pF
C501
220uF
R501
1K
Q502
D507
R503
4K7
Q503
R504
5 6R
C502
100uF
TO THE
VERTICAL
SCANNING
COILS
C504
330pF
R510
15K
Q510
R506
1R
R508
33R
C503
330pF
Q504
Q506
Q505
D505
FROM FRAME
DRIVE CIRCUIT
-10V

Figure 50 : CA1 Vertical Output Stage

Vertical drive waveform comes from the differentiation circuit Q507, 508, which combines the two outputs from IC201 on pins 63 (VERT B) and 64 (VERT A).

From this stage the waveform including flyback pulse is fed to the base of Q506 which along with Q505 is connected in a Darlington configuration, providing a high gain stage.

The signal fed in at this point has a negative going flyback pulse generated from the differentiation amplifiers, this is caused by one of the waveforms being marginally different from the other, the result being a pulse which is used for the flyback generation.

At the collector of Q505 is a waveform with a positive going flyback pulse, effectively this device is connected as a class A output with R512, D502, R501, R503 and R508 as its collector load. This waveform is fed directly to the base of Q504 the first of the two output transistors. This is a PNP transistor connected as an emitter follower providing unity voltage gain and high (Hfe) current gain.

Further up the ladder on the Collector load of Q505 (junction of R503 & R501) is the feed to the base of the second output transistor Q502. Again this device is connected as an emitter follower providing the necessary current gain to fulfil the push pull action of this output stage. The two emitters of these devices are connected together by R504 and R505 two fusible resistors of low values which provide crossover cushioning and the necessary fusing action should something fail in the output.

Q509 is used for flyback boost switching. During the scanning period of the waveform Q503 and therefore Q510 are turned on, this results in Q509 being turned off.

Whilst this situation prevails the capacitors Q504 and 501 are able to charge from the +10V rail being connected at the negative plates to the -10V rail via D509 and Q510 (presently saturated). When the waveform completes scan and enters into the positive going flyback pulse (at Q505) the current through the collector load of Q505 falls dramatically, as a result of this the voltage across R503 falls turning off Q503 and Q510, the base of Q509 is now pulled up by R502 this saturates Q509 effectively connecting the lower plate of C514 to the +10V rail. As these two capacitors are already charged to 20V this enables the cathode of D501 to rise momentarily to +30v (+10V and +20V), this enables a large flyback pulse to be fed to the scan coils, at the end of which the capacitors are discharged.

Frame Scanning Coils

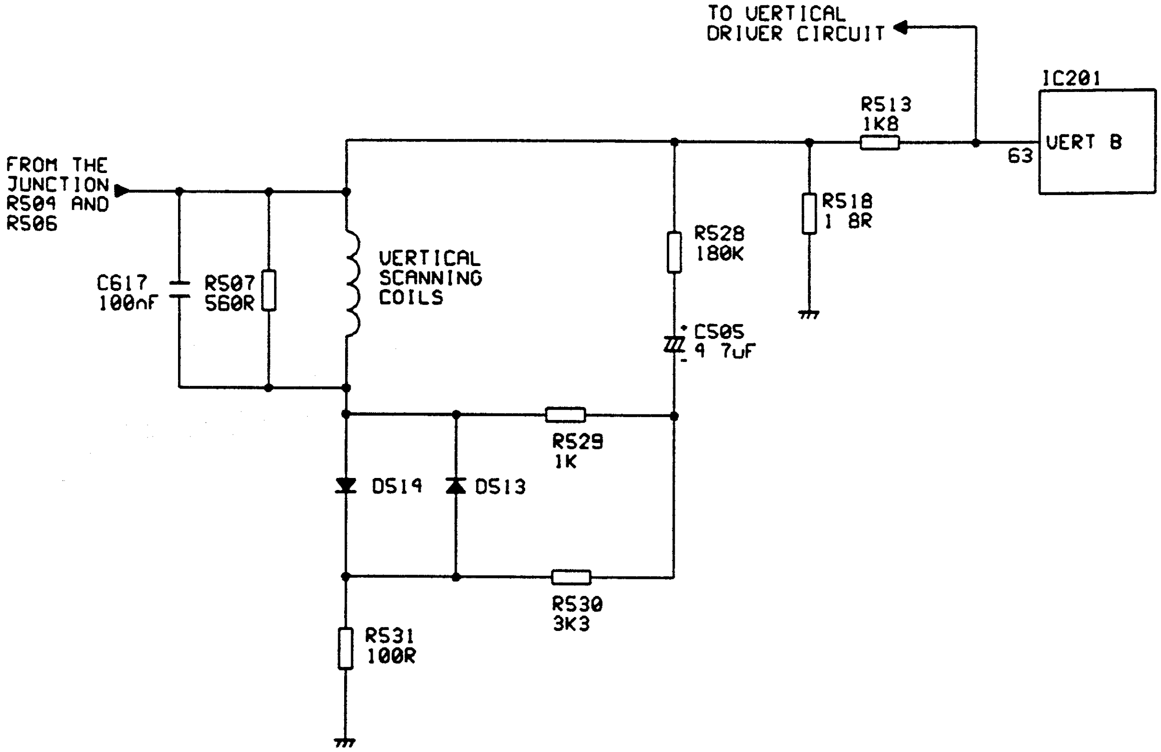

Figure 51 : CA1 Vertical Scanning Coils Circuit

CA1 Line Stage

Within this chassis, the line driver stage does not use a coupling transformer, but a push pull driver stage, which is similar in operation to that of the S3B chassis (DV5131H and DV5150H), however a few refinements have been made to the circuit.

Driver Stage

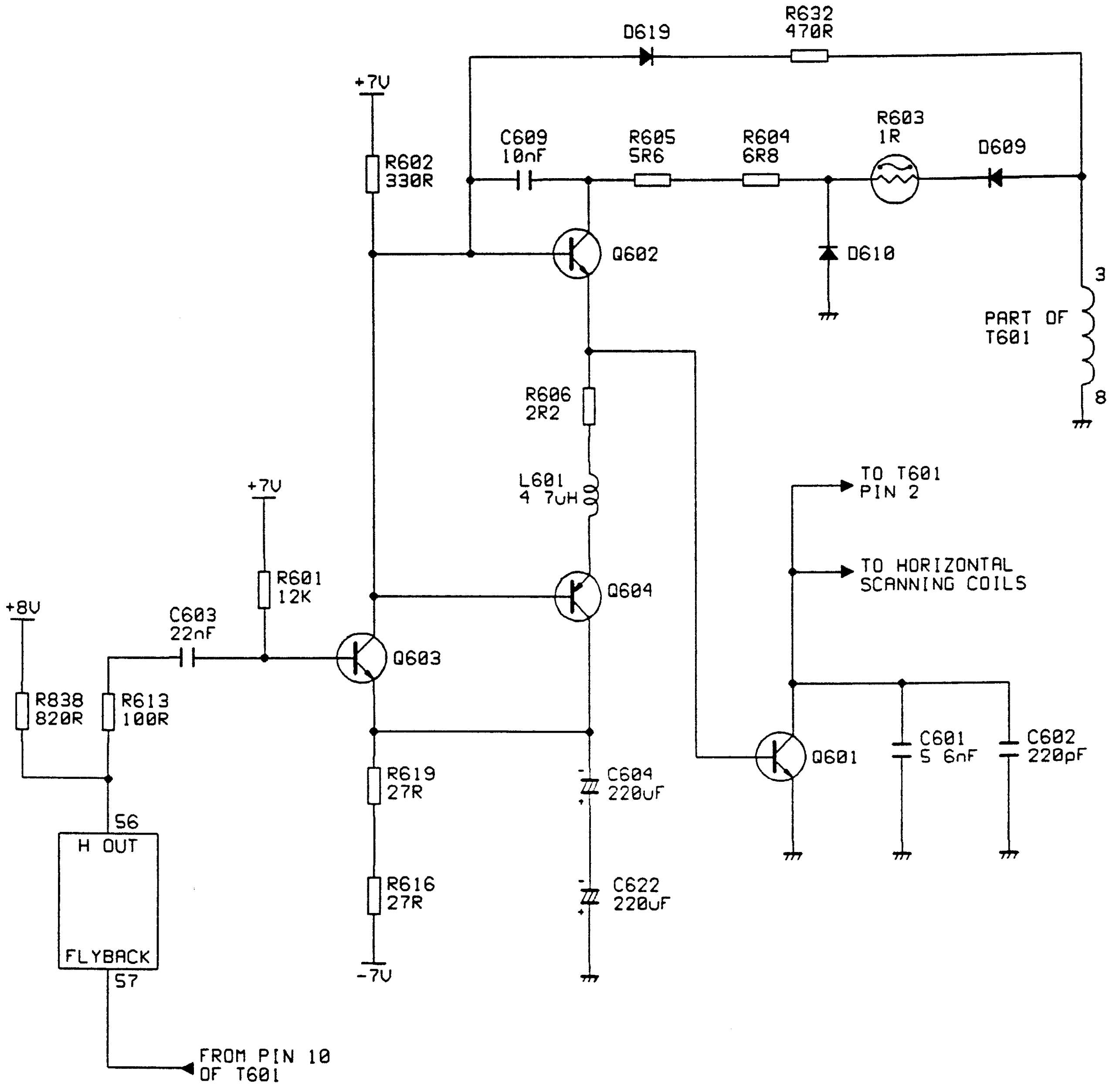
R632
470R
D619
+7V
C609
10nF
R605
5R6
R604
6R8
R603
1R
D609
R602
330R
Q602
D610
3
PART OF
T601
8
R606
2R2
L601
4 7uH
TO T601
PIN 2
+7V
R601
12K
Q604
TO HORIZONTAL
SCANNING COILS
+8V
C603
22nF
Q603
R838
820R
R613
100R
Q601
C601
5 6nF
C602
220pF
R619
27R
C604
220uF
S6
H OUT
R616
27R
C622
220uF
FLYBACK
S7
-7V
FROM PIN 10
OF T601

Figure 52 : CA1 Line Driver Stage

There are a number of similarities between the circuit shown above and that of the CA10. Firstly, there is no line driver (impedance coupling) transformer between the line driver and output transistor. Secondly, the low impedance source for driving the output transistor during its on condition is provided by a winding on the line output transformer.

As the receiver starts up the base of Q603 goes high, its emitter will drop and this will allow Q604 to turn on and Q602 to turn off. In this condition current will flow through Q604 and R619/R616 to the -10V supply and Q601 will be turned off. When the voltage on the base of Q603 drops, its emitter will go high and turn on Q602 and turn off Q604. This will allow current to flow from the +7V supply (via D619, R632, D609, R603/4/5 and the collect/emitter junction of Q603. Q601 will now turn on and current will flow in the primary winding of the line output transformer.

A pulse is fed back from pin 10 of T601 to indicate to the line time base generator that the stage has started up. At this point the drive signal changes frequency from 32.25 kHz (twice line frequency) to its normal running frequency of 15.625 kHz. Also at this time, to enable the output transistor to draw enough current to maintain its secondary voltages, its base current must increase significantly. As there is not enough power in the +7V supply to achieve this, so a tap is taken from T601 (winding 3 to 8) which feeds into the collector of Q602. This will provide a low impedance source, thus ensuring adequate current flow.

It is also important to turn off Q601 quickly to prevent it overheating and failing (note that on the 37cm versions of this chassis, the line output transistor is not fitted with a heat sink). When the line rate changes it is imperative that this is achieved, but just relying on the -10V supply via R616/9 is not enough, as this supply can not supply adequate current over the very short time it is required to maintain the voltage. To provide a lower impedance path, C604 and C622 are fitted. These capacitors allow the current and therefore voltage to be maintained on the collector of Q604 while Q601 turns off. As this off time is of a relatively short duration, the charge on the capacitors is not reduced significantly. During the on time of Q601 the charge on C604 and C622 is replenished via R619 and R616 from the -10V supply.

It is important that Q602 and Q604 do not turn on at the same time as could lead to the failure of the output transistor due to it working in the linear part of its characteristic. To eliminate this possibility, L601 is fitted to slow down the change of voltage at the base of Q601.

CA1 CRT Drive Amplifier

Unlike the CA10 chassis, the CA1 does not use a single IC for driving the CRT cathodes, instead a discrete component amplifier is used. The diagram shown below shows the red channel only.

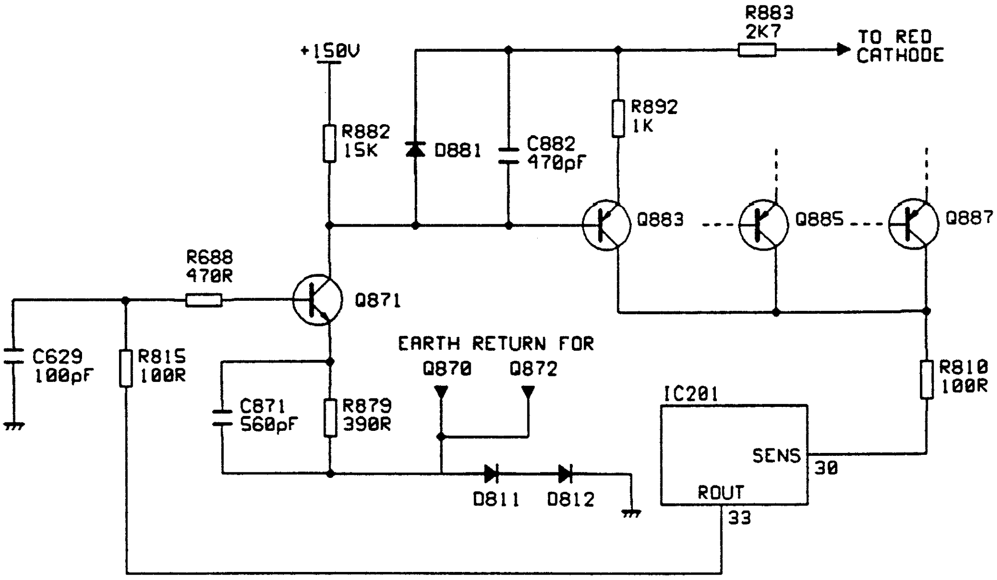
+150V
R883
2K7
TO RED CATHODE
R892
1K
R882
15K
D881
C882
470pF
Q883
Q885
Q887
R688
470R
Q871
C629
100pF
R815
100R
EARTH RETURN FOR
Q870 Q872
C871
560pF
R879
390R
D811 D812
R810
100R
IC201
SENS
30
ROUT
33

Figure 53 : CA1 CRT Drive Amplifier

CA1 Audio Output Amplifier

To enable the CA1 chassis to reproduce audio signals through a conventional loudspeaker, a linear push-pull amplifier is used. The circuit diagram is shown below.

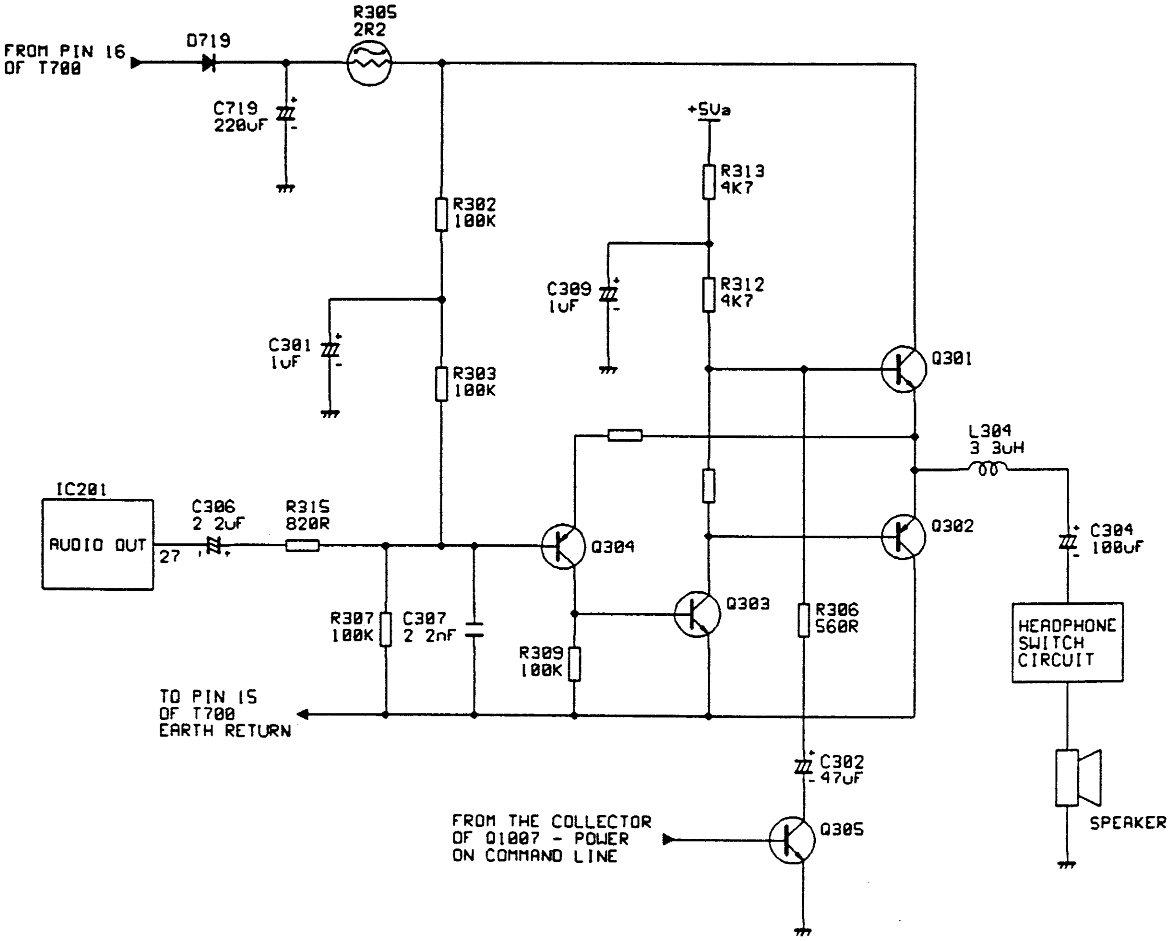
R305
2R2
FROM PIN 16
OF T700
D719
C719
220uF
+5Va
R313
4K7
R302
100K
C309
1uF
R312
4K7
C301
1uF
R303
100K
Q301
L304
3 3uH
IC201
AUDIO OUT
27
C306
2 2uF
R315
820R
Q304
Q302
C304
100uF
R307
100K
C307
2 2nF
Q303
R306
560R
R309
100K
HEADPHONE
SWITCH
CIRCUIT
TO PIN 15
OF T700
EARTH RETURN
C302
47uF
FROM THE COLLECTOR
OF Q1007 - POWER
ON COMMAND LINE
Q305
SPEAKER

Figure 54 : CA1 Audio Amplifier Circuit

CA1 Service Set Up Mode

To adjust the preset values contained within the NVM it is first necessary to enter the Service Mode, this is described below :-

1. Ensure that the receiver is on and displaying a picture, then switch it off using the mains switch.
2. Press the volume down button and the channel up button simultaneously.
3. Whilst still holding down the above buttons, switch the receiver on using the mains switch. Continue holding the buttons until a picture appears.
4. When the picture appears, the set will be in the service mode, release the buttons.

It is now possible to adjust the following settings :-

Horizontal Shift
Vertical Shift
Vertical Amplitude
Vertical Slope
Chrominance/Luminance Delay
Red Gain
Green Gain
Blue Gain
NVM Codes (see the **CA1 Non Volatile Memory Codes** section of these notes)

To change the setting mode, press the channel up or down button on the remote control of front of the television. To adjust the setting use the volume up or volume down buttons. When the adjustment is completed, the value will be automatically stored in the memory. Note that the NVM codes do not set this way.

There are four adjustments that are recommended to be carried out with reference to the service manual. These are :-

1. PIF/AGC Adjustment.
2. RF AGC Cut in Adjustment (I^2C Bus).
3. Focus Adjustment.
4. G2 Adjustment.

CA1 Non Volatile Memory Codes

All user setting are contained within the non volatile memory, IC1002 including a number of pre-set receiver parameters. Although these are pre-set for the model, they can be changed. Under normal circumstances this would serve no purpose, as the circuitry to preform the various functions may not be fitted. However, should a data corruption occur, or there is a need to modify the software, the locations and functions are shown below. At the end of this section an explanation is given on how to set these codes.

CA1 NVM Locations and Functions

Address (HEX)	Description	Default Value
00	Red Colour Temperature	
01	Green Colour Temperature	
02	Blue Colour Temperature	
03	Vertical Shift	
04	Horizontal Shift	
05	Vertical Amplitude	
06	Vertical Slope	
07	Luminance Delay - PAL	
08	Luminance Delay - SECAM	
09	S-Correction	
0A	Automatic Gain Control	
0B	Bit 0 : Bit 1 : 0 = No Front AV Sockets Fitted, 1 = Front AV Socket Fitted Bit 2 : 0 = Tuning Unlocked, 1= Tuning Locked (Hotel Mode) Bit 3 : 0 = All Band Tuning, 1= UHF Band Tuning Only Bit 4 : 0 = PAL System Only, 1 = PAL and SECAM Systems Bit 5 : 0 = Child Lock Disabled, 1 = Child Lock Activated Bit 6 : 0 = Manual Tuning, 1 = Automatic Tuning Bit 7 : 0 = OSD Symbols, 1 = OSD in English	
0C	AFT Adjustment Value for B/G and L Systems	
0D	AFT Adjustment Value for L' System	
0E	Maximum Volume Limit	
0F	Firm	
10	Red Colour Temperature	
11	Green Colour Temperature	
12	Blue Colour Temperature	
13	Vertical Shift	
14	Horizontal Shift	
15	Vertical Amplitude	

16	Vertical Slope	
17	Luminance Delay - PAL	
18	Luminance Delay - SECAM	
19	S-Correction	
1A	Automatic Gain Control	
1B	Bit 0 : Bit 1 : 0 = No Front AV Sockets Fitted, 1 = Front AV Socket Fitted Bit 2 : 0 = Tuning Unlocked, 1= Tuning Locked (Hotel Mode) Bit 3 : 0 = All Band Tuning, 1= UHF Band Tuning Only Bit 4 : 0 = PAL System Only, 1 = PAL and SECAM Systems Bit 5 : 0 = Child Lock Disabled, 1 = Child Lock Activated Bit 6 : 0 = Manual Tuning, 1 = Automatic Tuning Bit 7 : 0 = OSD Symbols, 1 = OSD in English	
1C	AFT Adjustment Value for B/G and L Systems	
1D	AFT Adjustment Value for L' System	
1E	Maximum Volume Limit	
1F	Firm	
20	Red Colour Temperature	
21	Green Colour Temperature	
22	Blue Colour Temperature	
23	Vertical Shift	
24	Horizontal Shift	
25	Vertical Amplitude	
26	Vertical Slope	
27	Luminance Delay - PAL	
28	Luminance Delay - SECAM	
29	S-Correction	
2A	Automatic Gain Control	
2B	Bit 0 : Bit 1 : 0 = No Front AV Sockets Fitted, 1 = Front AV Socket Fitted Bit 2 : 0 = Tuning Unlocked, 1= Tuning Locked (Hotel Mode) Bit 3 : 0 = All Band Tuning, 1= UHF Band Tuning Only Bit 4 : 0 = PAL System Only, 1 = PAL and SECAM Systems Bit 5 : 0 = Child Lock Disabled, 1 = Child Lock Activated Bit 6 : 0 = Manual Tuning, 1 = Automatic Tuning Bit 7 : 0 = OSD Symbols, 1 = OSD in English	
2C	AFT Adjustment Value for B/G and L Systems	
2D	AFT Adjustment Value for L' System	
2E	Maximum Volume Limit	
2F	Firm	
30	Table Long	

31	Firm	
32	Aging on. Automatic Switch on	
33	Switch on Delay Time	
34	Volume Setting	
35	Contrast Setting	
36	Colour Setting	
37	Brightness Setting	
38	Peaking (range 03-FH)	
39	Actual Programme	
3A	TV State, On or Off	
3B	Hue	
3C	Contrast Factory Preset	
3D	Colour Factory Preset	
3E	Brightness Factory Preset	
3F	Peaking Factory Preset	
40	On Timer Last Value	
41	Off Timer Last Value	
42	OSD State Bit 0 : Picture Normal On/Off Bit 1 : SCART/AV Locked Bit 2 : Frontal Locked Bit 3 : Row 8/30 Perm. (Reserved-Programme Internally) Bit 4 : 0 = PIN Does Not Appear, 1 = PIN Does Appear Bit 5 : Clock State (programmed internally) Bit 6 : Eliminate White Bars From Menus Bit 7 : 0 = On Timer, 1 = Real Timer and Alarm	
43	BKGD User's Correction	
44	BKGD User's Correction Preset Value (Normalised)	
45	Voltage Limit Between L'-L System (MSB)	
46	Voltage Limit Between L'-L System (LSB)	
47	Horizontal OSD Offset Bit 0 to Bit 5 : Offset Value Bit 6 : Don't Care Bit 7 : Direction Sign - 0 = Increase, 1 = Decrease	
48	Programme Search Speed All Band - High Nibble Complemented	
49	Programme Search Speed VHL Band - High Nibble Complemented	
4A	Programme Search Speed VHL Band - High Nibble Complemented	
4B	Programme Search Speed VHH Band - High Nibble Complemented	

4C	Channel Range in Factory Auto Install	
4D	Password - 0 = Off, 1 = On	
4E	Password First Digit	
4F	Password Second Digit	
50	Password Third Digit	
51	Password fourth Digit	
52	Free	
53	OSD Word 1 Bit 0 : OSD Program Size - 0 = Large (14"), 1 = Short (21") Bit 1 : OSD Program Displayed Time - 0 = Short Time, 1 = Long Time	
54	Red Reference for Auto BKGD Adjustment	
55	Green Reference for Auto BKGD Adjustment	
56	Blue Reference for Auto BKGD Adjustment	
57	Control 2 : OSO, VSD, CB, BLS, BKS, CS1, CS0, BB	
58	Control 3 : HOB, BPS, ACL, CMB, AST, CL2, CL1, CL0	
59	Vertical Zoom	
5A	Vertical Scroll	
5B	Control 0 : INA, INB, INC, CCC-D, FOA, FOB, XA, XB	
5C	Control 1 : FORF, FORS, DL, STB, POC, CM2, CM1, CM0	
5D	Control 5 : EVG, HCO, LBM, VID, STM, NCIN, VIM, AKB	
5E	Control 6 : IFS, AFW, IE1, COR, RBL, MAT, PRD, SBL	
5F	Control 7 : EVSINC, EBS, FFI, HBL, GAI, IE2, DS, DSA	
60	Not Used	
61-FF	Programs 0-52	
100-18D	Programs 53-99	

Procedure for Programming the NVM

To enable the various NVM locations to be changed it is necessary t0 enter the service mode as first. This is described below :-

1. Ensure that the receiver is on and displaying a picture, then switch it off using the mains switch.
2. Press the volume down button and the channel up button simultaneously.
3. Whilst still holding down the above buttons, switch the receiver on using the mains switch. Continue holding the buttons until a picture appears.
4. When the picture appears, the set will be in the service mode, release the buttons.

To access the NVM memory, press the channel up button on the remote control until the NVM setting function is reached. Note that the NVM address is shown in green and the NVM value is shown in red.

Each of the NVM values are stored as a hexadecimal code, each code comprises of two hexadecimal numbers. Each of these numbers will break down into a four bit binary code.

Hex code	A	5
Binary code	1 0 1 0	0 1 0 1
Button on remote to toggle	7 6 5 4	3 2 1 0

In the example given above, the hexadecimal code is A5, the binary equivalent is 1010 0101 and the remote control button to toggle each bit on or off, i.e. a 1 or a 0 is shown below the binary code. Therefore to change this to A6, remote control buttons 1 then 0 would be pressed.

NVM Programming Application

One application for entering the NVM set up mode is to enable the Hotel Mode as described below.

To block the tuning mode NVM address 0B has to be changed as follows.

Model	Nominal Value	Hotel Value
37DM23H	F8	FC
37DT25H	F8	FC
51DT25H	F8	FC

To set the maximum volume level, change NVM address 0E as follows.

Maximum volume	FF
90% volume (approximately)	E7 to EF
80% volume (approximately)	CF to DF
73% volume (approximately)	BF
62% volume (approximately)	9F to BF
50% volume (approximately)	7F

When the hotel mode has been set, turn off the receiver at the mains switch, turn back on and check all functions.

Future Developments

Sharp are currently developing two wide screen models to be introduced into the UK market place sometime at the start of 1998. These are the 76DW18H and 66DW18H models and will be fitted with the CA100 chassis.

Both receivers have the same specifications, except for CRT size. The basic specifications are as follows

* Dolby Pro Logic
* NICAM
* 100Hz digital scanning
* AI optical picture control
* 99 channel, auto sort tuning (UHF/VHF)
* Zoom modes and still image
* 90W (MPO)
* 3 rear mounted SCART sockets
* S-VHS input
* Front AV sockets
* Headphone socket
* Cabinet supplied with the receiver that includes centre speaker

It is also envisaged that future designs will incorporate a test signal (simple grid pattern) into the service mode to facilitate easier setting up of picture geometry.

Note :

Sharp reserve the right to make design and specification changes for product improvement.

Faults

Notes